

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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First Named Inventor or Application Identifier:

Masaki UKAI

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231**

1. ☒ Fee Transmittal Form
2. ☒ Specification, Claims & Abstract [Total Pages: 63]
3. ☒ Drawing(s) (35 USC 113) [Total Sheets: 32]
4. ☒ Oath or Declaration [Total Pages: 3]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Copy
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ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) [] Power of Attorney
10. ☐ English Translation Document (if applicable)
11. ☒ Information Disclosure Statement (IDS)/PTO-1449 [] Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ☐ Small Entity Statement(s) [] Statement filed in prior application, status still proper and desired.
15. ☒ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. ☐ Other:

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:[] Continuation [] Divisional [] Continuation-in-part (CIP) of prior application No: / **18. CORRESPONDENCE ADDRESS**

STAAS & HALSEY, LLP
Attn: James D. Halsey, Jr.
700 Eleventh Street, N.W., Suite 500
Washington, DC 20001

Telephone: (202) 434-1500
Facsimile: (202) 434-1501

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)	
)	
Masaki UKAI)	
)	Group Art Unit: To Be Assigned
Serial No.: To Be Assigned)	
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Filed: March 20, 2000)	Examiner: To Be Assigned
)	
For: DEVICE AND METHOD FOR)	
CONTROLLING WRITING OF)	
BRANCH HISTORY INFORMATION)	

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Before examination of the above-identified application, please amend the application as follows:

IN THE CLAIMS:

Claim 8, lines 1 and 2, change "any one of claims 4 through 7" to --claim 1--.

Claim 15, line 1, change "claim 1 or 10" to --claim 1--.

Claim 39, line 1, change "claim 26 or 34" to --claim 26--.

REMARKS


This Preliminary Amendment is submitted to improve the form of the specification and claims as originally filed.

[illegible]

It is respectfully requested that this Preliminary Amendment be entered in the above-references application.

If any fees are required in connection with the filing of this Preliminary Amendment, please charge same to our Deposit Account No. 19-3935.

STAAS & HALSEY


James D. Halsey, Jr.
Registration No.: 22

James/D. Halsey, Jr.
Registration No.: 22,729

700 Eleventh Street, N.W.
Washington, D.C. 20001
(202) 434-1500

Date: March 20, 2000

[illegible]

Title of the Invention: DEVICE AND METHOD FOR
 CONTROLLING WRITING OF BRANCH
 HISTORY INFORMATION

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Field of the Invention

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prediction unit represented by a branch history is provided and the establishment of a branch is predicted. If a branch establishment is predicted, the performance could be improved by inputting an instruction on the branch destination following a branch instruction to an execution control unit or instruction process unit.

However, in a conventional branch prediction unit, the branch history information of a branch instruction of which the execution is completed in a branch control unit was registered in a branch history by temporarily stopping the instruction fetch.

According to this system, in particular, if a branch prediction fails and a correct subsequent instruction is re-executed, and specifically, if a re-instruction fetch occurs, an instruction fetch pipeline is temporarily stopped by the branch history information writing the completed branch instruction into the branch history although the frequency of a fetch request is high since a temporary instruction buffer is empty. Accordingly, the performance was not improved.

Specifically, although, as in the execution of a branch instruction BC shown in Fig. 1, in the cycle W of the execution cycle of a branch instruction, the

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Summary of the Invention

An objective of the present invention is to provide an instruction execution control device for suppressing a process delay in an information processing apparatus provided with a branch prediction unit, and a method thereof.

A device in the first aspect of the present invention comprises a control unit controlling in such a way that the writing of branch history information into a branch prediction unit and the control over the memory unit may not occur simultaneously in a branch history information write control device in an instruction execution processing apparatus provided with a memory unit storing an instruction string, etc., and a branch prediction unit performing the branch prediction of a branch instruction.

In a branch history information write control device of an instruction execution processing apparatus provided with a branch prediction unit performing the branch prediction of a branch instruction, a device in the second aspect of the present invention comprises a return address stack unit and a control unit controlling in such a way that if the branch instruction is not executed although the branch instruction is an instruction corresponding to

a sub-routine call or return, and the write request of the branch history information of the branch instruction is issued to the branch prediction unit, the branch history information is written in the
5 branch prediction unit, but the return address stack unit may not be operated.

A method in the first aspect of the present invention is an instruction control method in an apparatus provided with a memory storing an
10 instruction string, etc., and a branch prediction unit performing the branch prediction of a branch instruction, and comprises the step of controlling in such a way that the writing of branch history information in the branch prediction unit and the
15 control over the memory may not occur simultaneously.

A method in the second aspect of the present invention is an instruction control method in an apparatus provided with a branch prediction unit performing the branch prediction of a branch
20 instruction and a return address stack, and comprises the step of controlling in such a way that if the branch instruction is not executed although an instruction corresponding to the sub-routine call or return obtained as an execution result of the branch
25 instruction issues the write request on the branch

history information to the branch prediction unit, the branch history information is written in the branch prediction unit, but the return address stack is not operated.

5 Although conventionally an instruction fetch is held and branch history information is written in the branch prediction unit (branch history), according to the present invention, an instruction fetch is not held and the branch history is written in a branch
10 history in a timing such that the writing of the branch history information in the branch history and the control of the instruction fetch, etc., over a memory may not occur simultaneously. Accordingly, no instruction fetch is held and thereby the execution
15 process speed can be improved.

Brief Descriptions of the Drawings

Fig. 1 shows conventional problems occurring at the time of execution of a branch instruction.

20 Figs. 2A and 2B show conventional problems occurring when a short loop is formed between branch instructions.

Fig. 3 shows effects obtained when a branch instruction is executed according to the present
25 invention.

Figs. 4A and 4B show effects obtained when a short loop is formed between branch instructions according to the present invention.

5 Fig. 5 shows the basic configuration of the preferred embodiments of the present invention.

Fig. 6 shows an example configuration of a branch history.

10 Fig. 7 shows an example basic configuration for delaying the writing of the branch history information of a branch instruction re-instruction-fetched.

Fig. 8 shows an example detailed configuration of a block 31 shown in Fig. 7.

Fig. 9 shows an example detailed configuration of a block 32 shown in Fig. 7.

15 Fig. 10 shows an example of a circuit corresponding to a block 30 shown in Fig. 7.

Fig. 11 is a timing diagram of a preferred embodiment using a counter.

20 Fig. 12 shows another preferred embodiment of a circuit corresponding to a box 30 shown in Fig. 7.

Fig. 13 shows an example circuit configuration for operating the device even if a temporary instruction buffer is empty.

25 Fig. 14 shows another preferred embodiment of a circuit of a box 30 shown in Fig. 7 (No. 1).

a write reservation station.

Fig. 25 shows an example configuration of a reservation station in the case where writing in a reservation station is available after the completion of an instruction execution under IID (Instruction ID) control.

Fig. 26 shows an example configuration of the CSE valid circuit of a write reservation station.

Fig. 27 shows the data storage configuration of a write reservation station.

Fig. 28 shows an example configuration of a CSE valid circuit in the case where a branch prediction unit is provided with a return address stack.

Fig. 29 shows an example circuit for nullifying the entry of a reservation station if an instruction execution is temporarily stopped due to an interruption, etc.

Fig. 30 shows one preferred embodiment of a bypass hit circuit.

Description of the Preferred Embodiments

In the preferred embodiment of the present invention, the writing of branch history information is held while a branch history is being looked up, and the branch history information is written in a cycle

which does not look up the branch history. If this method is used, any impediment of an instruction fetch disappears. Accordingly, a pipeline process can be smoothly performed and thereby the degradation of the performance described earlier can be prevented.

Specifically, as shown in Fig. 3, if an instruction string shown in Fig. 1 is executed, in this preferred embodiment, an instruction fetch of NOP5, which was conventionally started following the cycle W of a branch instruction BC, can be started in the same cycle as the cycle W of the branch instruction BC. Accordingly, by adopting this preferred embodiment, the performance can be improved by one clock cycle on average.

While the density of an instruction fetch is high immediately after a re-instruction fetch, writing into a branch history is held. In particular, since a new branch instruction is executed and completed for several clock cycles immediately after a re-instruction fetch, most of performance degradation can be prevented in a small-scale circuit without providing a reservation station described next.

The preferred embodiment of the present invention provides a method for realizing a temporary buffer in order to hold the writing of branch history

information. If instruction fetch requests continue, and, even if an instruction pipeline process is very smoothly executed, the impediment of an instruction fetch request can be eliminated by providing a reservation station as a holding device for realizing such a buffer function. Accordingly, the performance degradation can be prevented.

If there is a new write request while branch history information is being held by the holding device, a control method for preventing a reservation station which becomes a temporary buffer, from overflowing is provided. According to such a preferred embodiment, all branch history information can be registered/updated in a branch history without failure.

Depending on the configuration of a branch history, a plurality of branch histories can be simultaneously written in the same cycle. In a branch history comprised of a plurality of RAMs (random access memory) which can store another entry, a maximum of the same number of different entries as RAMs composing the branch history can be written. It is clear that by doing so, a lot of history information of branch instructions can be written in a branch history while the impediment of writing for

branch prediction is reduced.

Branch history information is reported before a branch instruction is completed. Generally speaking, in an instruction execution control device adopting a system, such as an out-of-order, etc., the branch instruction is sometimes held because the previous instruction is not completed yet although all conditions for executing a specific instruction are met. In particular, in this case, after the uncompleted instruction meets all conditions, instructions which have been held are collectively attempted to be completed. Accordingly, by adopting such a method, the load of writing in the branch history can be dispersed.

If in the case of a branch prediction unit provided with a return address stack, the return address stack is operated when the branch history information of a branch instruction which has not actually been executed is reported, the correspondences between pairs of subsequent sub-routine calls and returns naturally collapse, and the prediction of the branch destination address of a sub-routine return instruction fails. Therefore, the return address stack is configured not to be operated by the call/return instruction mistakenly being

executed as long as the return address stack is actually executed, although the branch instruction is registered in a branch history.

5 The registration/update of the branch history information is held until an instruction execution is completed. In this case, the branch history information can be written simultaneously with the execution completion or the writing can be held until there is a favorable timing. In this case, 10 alternatively, a method for identifying an instruction with an ID number assigned for each instruction can be used to judge whether the execution of the branch instruction is completed. If the execution of the branch instruction is cancelled although the branch history information is transmitted, the relevant entry 15 corresponding to the write reservation station can also be nullified. In this case, since the history information of a branch that has been executed with certainty is to be used if the writing is held until 20 the execution is completed, no incorrect branch history information is registered and thereby the accuracy of a branch prediction is improved.

 If a branch prediction is performed by a branch prediction unit, branch history information, writing 25 of which is held, etc., can also be used by bypassing

the writing. In this case, since bypassing was performed, the latest branch history information can be used, and an enhanced effect can be obtained, in particular in a local loop. Specifically, the process
5 delay of a pipeline can be improved by approximately several clock cycles for each short loop.

For example, if, as shown in Figs. 4A and 4B, short loops shown in Figs. 2A and 2B are executed, conventionally, as shown in Figs. 2A and 2B, the
10 instruction fetch of the instruction L(3) of the third loop is started in a cycle B of the execution cycle of the instruction L(2) of the second loop. However, in Figs. 4A and 4B, the instruction fetch of the instruction L(3) is started in the timing of the cycle
15 IB of the instruction L(2) by bypassing the writing and using the branch history information. In this way, according to this preferred embodiment, performance can be improved by six clock cycles compared with the conventional method shown in Figs. 2A and 2B.

20 As the RAMs of a branch history, dual port RAMs which can perform writing and reading independently in the same cycle, are used. If there is room in circuit mounting, the performance degradation can be prevented most easily using this method.

25 Fig. 5 shows the basic configuration of the

preferred embodiments of the present invention.

The instruction execution control device of the present invention adopts an out-of-order system. Therefore, in Fig. 5, which concerns an execution control unit, only approximate time dependency is shown.

In this preferred embodiment, it is assumed that an instruction fetch can secure an instruction string of 16 bytes which is 8-byte-aligned, at one request.

First, the address of an instruction to be fetched next is inputted to a selector 11. The addresses to be inputted to the selector 11 are the sequential instruction address which is inputted from an adder 10, the start address for an interruption process, the prediction branch destination instruction address which is the branch prediction result inputted from a branch history, and the branch destination instruction address which is confirmed by a branch instruction process unit 17 executing a branch instruction. The selector 11 is controlled by an instruction execution flow control device (not shown in Fig. 5) which is controlled by an instruction completion process unit 19 for guaranteeing the order of instructions in an out-of-order type information processing apparatus, and is configured to select an

appropriate address in each case. The address
outputted from the selector 11 is inputted to a branch
history 20 as the effective address IF_EAG of the
instruction fetch, and simultaneously is inputted to
5 an instruction fetch address register 12 to perform
the instruction fetch. The instruction fetch address
register 12 inputs an instruction corresponding to the
address given by the selector 11, and simultaneously
the address of the instruction is inputted to the
10 adder 10. After being stored in a temporary
instruction buffer 14, the instruction inputted to an
instruction cache 13 is decoded in a decoder 15 and
transmitted to the branch instruction process unit 17,
an execution instruction process unit 18, and other
15 instruction process units to be processed. In the case
of a branch instruction, the execution of branch
conditions, etc., is performed in an address
calculating unit 16, and the result is inputted to the
branch instruction process unit 17. If the branch
20 instruction of the execution is not determined and the
execution is described by means of an instruction
string, the execution is performed by the execution
instruction process unit 18, and the execution result
is inputted to the branch instruction process unit 17.
25 Furthermore, the execution completion reports of the

branch instruction process unit 17 and execution instruction process unit 18 are processed by an instruction completion process unit 19, and are used to guarantee an instruction execution order and to control an out-of-order type instruction execution order. The address of a branch destination instruction which is determined as an execution result of the branch instruction is inputted to the selector 11 from the branch instruction process unit 17.

Fig. 6 shows an example configuration of a branch history.

The branch history 20 is comprised of two RAMs 20-1 and 20-2, and these two RAMs 20-1 and 20-2 are configured to search for branch history information in the ranges of high-order 8 bytes and low-order 8 bytes, respectively, using an 8-byte-aligned instruction fetch address. According to this preferred embodiment, the branch history 20 is provided with a return address stack to predict the return destination of a sub-routine return instruction, which is not shown in Fig. 6.

According to this preferred embodiment, the branch instruction process unit 17 in the execution process unit can handle a maximum of four branch instructions, a maximum of one out of four branch

instructions is simultaneously prepared for the execution completion, and the branch instruction is transmitted to the instruction completion control unit 19. According to the prior art, branch history information was transmitted to the branch history in this timing.

The instruction completion control unit 19 assigns IIDs to all instructions being executed (from instruction decoding until completion), and manages the execution. In this preferred embodiment, it is assumed that a maximum of 16 instructions can exist in the execution unit. Specifically, it is assumed that any value between 0 and 15 is assigned as the value of the IID.

It is preferable to use as the branch history dual port RAMs which can perform reading and writing simultaneously.

Fig. 7 shows an example basic configuration for delaying the writing of the branch history information of a branch instruction re-instruction-fetched. Figs. 8 and 9 show example detailed configurations of the blocks 31 and 32 shown in Fig. 7.

According to this preferred embodiment, if it is found in the branch instruction process unit 17 that a branch prediction has failed, the branch instruction

process unit 17 issues a correct branch destination address (or subsequent instruction address) and makes a request for a re-instruction fetch.

At this time, if an instruction cache 13 cannot
5 accept the request for some reason, the re-instruction
fetch request is held until the request can be
accepted. While the re-instruction fetch request is
being held, +REIFCH_REQUEST remains ON. In this case,
usually this signal is directly inputted to the block
10 30. However, a circuit shown in Fig. 13, which is
described later, is provided and a signal outputted
from this circuit can also be inputted to the block
30 instead.

In this case, there is a possibility that the
15 timing of issuing the request and the timing of
writing into the branch history may match. In that
case, according to the prior art, priority is given
to writing into the branch history 20, and the re-
instruction fetch request is further delayed by one
20 or more clock cycles. According to this preferred
embodiment, since priority is, without fail, given to
the re-instruction fetch request, conventional
performance degradation does not occur.

If the re-instruction fetch request
25 (+REIFCH_REQUEST of "H") is inputted to the block 30,

both a signal obtained by logically inverting a signal for holding the writing of branch history information in the branch history 20 (-WAIT_BR_COMP_WRITE) and a signal for holding the re-instruction fetch signal of a re-instruction fetch (+BR_COMP_REIFCH_HOLD) are outputted. +BR_COMP_REIFCH_HOLD is inputted to the block 31. -WAIT_BR_COMP_WRITE is inputted to the block 32. The block 31 receives branch information, such as +BR_COMP_AS_TAKEN, etc., and further, a branch instruction address (+BR_COMP_IAR) and a branch destination instruction address (+BR_COMP_TIAR) are inputted to the block 31. Then, a signal for controlling an instruction to write in the branch history (+CREATE_NEW_ENTRY, +UPDATE_OLD_ENTRY, +ERASE_ENTRY), branch history information, a signal obtained by latching a branch destination instruction address (+BR_COMP_IAR_LCH), and a signal obtained by latching a branch destination instruction address (+BR_COMP_TIAR_LCH) are outputted from the block 31. The branch history information and branch destination instruction address are inputted to the port for writing data of the branch history 20. The branch instruction address is inputted to the selector 34 together with an instruction fetch address (+IF_EAG). A signal for instructing to write in the branch

history 20 is outputted from the block 32. By this signal, an appropriate address is outputted from the selector 34. Simultaneously, the branch history 20 is made to enter a writable state, and the branch history information, etc., can be written.

Fig. 8 shows an example circuit detail of the block 31 shown in Fig. 7, which stores data while writing is being held up.

A signal obtained by logically inverting a signal indicating whether the update of the entry of the branch history 20 is valid (-BRHIS_UPDATE_VALID) and +BR_COMP_REIFCH_HOLD are inputted to an AND circuit 41. Therefore, if the update of the entry of a branch history is invalid and a re-instruction fetch is requested, branch history information, a branch instruction address and a branch destination instruction address are stored in a latch circuit 42. The branch history information, branch instruction address and branch destination instruction address are outputted from the latch circuit 42. As described with reference to Fig. 7, simultaneously, +CREATE_NEW_ENTRY, +UPDATE_OLD_ENTRY, +ERACE_ENTRY, which are signals for instructing to write in the branch history 20, are extracted from the branch history information and are outputted from the latch

(see Fig. 11(d)), writes branch history information in a branch history (see Fig. 11(e)) and returns to an execution waiting (re-instruction fetch request waiting) state. Since by using this method, priority is given to these three instruction fetch requests over a normal re-instruction fetch, this method is applicable to a case where the temporary instruction buffer 14 is empty as well as to a temporary instruction fetch request. In this case, an output shown in Fig. 13 can be inputted instead of a signal +REIFCH_REQUEST, which is one of the input signals shown in Figs. 7 and 10.

Specifically, the counter shown in Fig. 10 is comprised of two bits, and if +REIFCH_REQUEST is inputted, a signal of positive logic and a signal of inverted logic are inputted to one terminal of an AND circuit 61 and one terminal of an OR circuit 62, respectively, via a latch circuit 60. In Fig. 10, <0> is a high-order bit and <1> is a low bit. If a re-instruction fetch signal is "H", the value stored in a latch circuit 63 becomes "01", and is maintained. If the re-instruction fetch signal becomes "0", "0" and "H" are outputted from the terminal Q of the latch circuit 60 and the inverted terminal of Q, respectively. Therefore, if a counter value "01" is

Then, if the count value becomes "3" two clock cycles later, the re-instruction fetch hold signal (+BR_COMP_REIFCH_HOLD) and the signal for permitting to write in the branch history 20 (+WRITE_BRHIS_VALID) become "L" and "H", respectively, and thereby writing in the branch history becomes available.

Fig. 12 shows another preferred embodiment of a circuit corresponding to the box 30 shown in Fig. 7.

In Fig. 12, if a valid instruction is decoded in an instruction decoder 15, a signal +D_VALID becomes ON. The re-instruction fetch signal (+REIFCH_REQUEST) and a signal +D_VALID are provided to a set/reset flip-flop 81 as a set signal and a reset signal, respectively. In this way, the output signal of this flip-flop 81 is maintained from when a re-instruction fetch request is issued until an instruction string corresponding to the request is decoded. Therefore, while the output signal of the flip-flop is ON, the signal +BR_COMP_REIFCH_HOLD is ON, and -WAIT_BR_COMP_WRITE (+BR_COMP_WRITE), which is a signal obtained by inverting a signal outputted from an inverter 82 becomes OFF.

Fig. 13 shows an example circuit configuration for operating the device even if a temporary instruction buffer is empty.

A circuit shown in Fig. 13 provides a signal which replaces +REIFCH_REQUEST, as the input of the box 30 shown in Fig. 7. Specifically, (1) if an instruction buffer 14 is empty (+I_BUFF_EMPTY is "H"),
 5 (2) if in a cycle IT, an instruction fetch request is invalid (-IT_IF_REQ_VALID is "H") and (3) if in a cycle IB, the instruction fetch request is invalid (-IB_IF_REQ_VALID is "H"), the output of an AND circuit 91 becomes "H". Therefore, if the three conditions,
 10 (1) to (3), above are met or if there is a re-instruction fetch request (+REFECH_REQUEST is "H"), a signal +REIFCH_REQ_OR_IF_EMPTY becomes ON. Then, this signal is inputted to the box 30 shown in Fig. 7 instead of a re-instruction fetch signal.

15 Figs. 14 and 15 show another preferred embodiment of the box 30 shown in Fig. 7.

Fig. 14 shows an example configuration of the box 30 in the case where if there is a re-instruction fetch, branch history information is not written in the branch history 20, but if the instruction cache 13 cannot accept an instruction fetch, the branch history information is written in the branch history 20. In this case, not an instruction fetch request, but a signal +SU_BUSY, which is transmitted from the
 20 instruction cache 13, is inputted as input. The fact
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signal as a hold signal, branch prediction data (branch history information) is held.

If a reservation station 120 (120-1) shown in Fig. 16 is used, writing in the branch history 20 can also be controlled by using one of the preferred embodiments described above.

The reservation station 120 is comprised of four entries (RSW0-RSW3). In each entry RSWx (x=0-3), a valid flag (Valid) and an instruction address (IAR) are registered, and further branch history information 121 corresponding to the registered instruction is stored.

Fig. 17 shows the overall circuit configuration of a preferred embodiment which controls writing in the branch history 20 in the case where the reservation station 120 shown in Fig. 16 is used.

First, branch history information (+BR_COMP_AS_TAKEN, etc.) is inputted to the reservation station 120 by the branch instruction execution unit, and simultaneously both a branch instruction address (+BR_COMP_IAR) and a branch destination instruction address (+BR_COMP_TIAR) are also inputted. The reservation station 120 is configured as shown in Figs. 16 and 22-25. From the reservation station 120, data to be written in a

branch history for odd addresses 20-1 and a branch history for even addresses 20-2 are outputted via a selector 130 shown in Fig. 21 (+BRW_ODD/EVEN_DATA). Signals outputted from the reservation station 120 are processed in a block 140 to generate an odd address branch history write permit signal (+RSW_ODD_WRITE_VAL) and an even address branch history write permit signal (+RSW_ODD_WRITE_VAL), respectively, which become signals for permitting to write in the branch histories 20-1 and 20-2, respectively. In a selector 150, either an address IAR transmitted from the reservation station 120 or an address for retrieving from the branch history 20 (+IF_EAG) is selected. In particular, if a write permit signal is received from the block 140, the selector 150 selects the IAR and makes a certain circuit write in the branch history 20. For example, the writing in the branch history 20 is performed by a circuit shown in Fig. 22.

In this preferred embodiment, plurally and simultaneous writing is also performed.

Figs. 16-20 show control circuits for plurally and simultaneously writing in the branch history 20.

In this preferred embodiment, the branch history is comprised of two RAMs. Therefore, if there are two

bytes and if there are 16 or more different write addresses, the addresses are written in the low-order 8 bytes and the high-order 8 bytes of the branch histories 20-1 and 20-2, respectively. Then, the device is controlled in such a way that the combinations of two addresses with priority are written in the branch history 20 with priority in a priority determination circuit 143. If the signal of one of the AND circuits 142-1 - 142-6 is ON, a plurally writable signal (+WRITE_DOUBLE) is outputted.

A circuit 140B located in the lower section of Fig. 18 is a write signal selection circuit used when one entry of the reservation station 120 is written into the branch history 20. If either of the valid signals of the entry of each reservation station RSWx is ON, a signal indicating that data to be written is available (+WR_DATA_AVAILABLE) is outputted. Priority is set to the writing of each entry of the reservation station 120 by a circuit 146. If a plurally writable signal is OFF and +WR_DATA_AVAILABLE is "H", a single write signal (+WRITE_SINGLE) is outputted and simultaneously a signal indicating which entry of the reservation station 120 should be written (+WRITE_RSWx) is outputted.

In Fig. 18, the output of this AND circuit can

also be used instead of the signal +RSW_x_VALID by providing an AND circuit 149 as shown in the upper left section of Fig. 18. In this case, the signal +RSW_x_VALID and a signal -RSW_CSE_VALID, which is described later, are inputted. After an instruction execution is completed, writing in the branch history 20 can be performed using these signals. Specifically, if the instruction is not completed, the signal +RSW_CSE_VALID is ON. How to generate this signal is described later.

Fig. 19 shows a selection circuit for plurally and simultaneously writing in a branch history (No. 2).

In Fig. 19, the output from the single write selection circuit 140B shown in Fig. 18 and the 28th bit of an instruction address (IAR) outputted from the reservation station 120 are inputted to AND circuits 151 (151-1 - 151-4). By checking whether a write signal inputted from the single write selection circuit and the 28th bit of an instruction address are ON or OFF, a write permit signal used when the instruction address is odd, is outputted. Then, if one of the AND circuits 151-1 - 151-4 is ON, the writing of an odd address is permitted. Therefore, if this signal is outputted, a signal for permitting to write

in the odd branch history 20-1 (+RSW_ODD_WRITE_VALID) is outputted. If the double write signal (+WRITE_DOUBLE) is ON, writing in the odd branch history 20-1 and even branch history 20-2 are permitted. Specifically, +RSW_ODD_WRITE_VALID and +RSW_EVEN_WRITE_VALID are turned ON. If the writing in the odd branch history 20-1 is OFF, a signal to be inputted to an AND circuit 66 becomes ON. Furthermore, if the single write signal (+WRITE_SINGLE) is ON, a signal for permitting to write in the even branch history 20-2 (+RSW_EVEN_WRITE_VALID) becomes ON. If either a signal indicating that writing in the branch history 20 is not held (-WAIT_BR_COMP_WRITE) or a signal for compulsorily writing in the branch history 20 (+FORCE_WRITE_BRHIS) is ON, this signal for permitting to write in the odd or even branch history is outputted. +FORCE_WRITE_BRHIS is described later.

Figs. 20 and 21 show selection circuits for plurally and simultaneously writing in branch histories (No. 3) (No. 4).

A circuit shown in Fig. 20 generates select signals for writing in the entries RSW0-RSW3 of the No. 1 through No. 3 branch histories of the reservation station 120 (+SEL_RSWx_WRITE) using the output shown in Fig. 18 as input, and inputs the

signals to a circuit shown in Fig. 21.

The circuit shown in Fig. 21 selects data transmitted from the reservation station 120 (RSW_x_DATA). In Fig. 21, a selection circuit for an odd branch history 20-1 and a selection circuit for an even branch history 20-2 are separately configured. Data from the reservation station 120 are inputted to multiplexers 181 and 182, and one of the pieces of data is transmitted as RSW_OLD_DATA or RSW_EVEN_DATA.

The multiplexer 181 adds a select signal (+SEL_RSW_x_WRITE), which is the output of the circuit shown in Fig. 20, to the 28th bit of an instruction address (IAR) inputted from the RSW0 to RSW3 of the reservation station 120, and switches the operation based on the result. In this way, if the select signal is ON and the instruction address is odd, a select signal is transmitted and corresponding data are transmitted.

In the same way, the multiplexer 182 adds a select signal, which is the output of the circuit shown in Fig. 20, to a signal obtained by logically inverting the 28th bit of an instruction address inputted from the RSW0 to RSW3 of the reservation station 120, and switches the operation based on the result. In this way, if the select signal is ON and

Furthermore, if in this preferred embodiment, the reservation station 120 is full and data to be written are further transferred from the branch instruction control unit, at least one piece of data being stored
 5 can be written. Figs. 23 and 24 show this preferred embodiment.

Fig. 23 shows an example circuit configuration of a circuit for compulsorily writing in a branch history.

10 If the valid signal of an entry from a circuit shown in Fig. 24 (+RSWx_VALID) is inputted to an AND circuit 201 and all the entries of all the reservation stations 120 are valid, the reservation stations are full. Therefore, in this case, a signal indicating
 15 this +RSW_FULL is outputted. If the update of the branch history 20 is valid, +BRHIS_UPDATE_VALID inputted from the branch instruction process unit 17 becomes ON, a signal for compulsorily writing in a reservation station +FORCE_WRITE_BRHIS is generated
 20 and used in the operation shown in Fig. 19.

Fig. 24 shows an example configuration of the valid circuit of a reservation station 120.

If the update of the branch history 20 is valid (+BRHIS_UPDATE_VALID is ON) and the entry RSW0 of the
 25 No. 1 branch histories of a reservation station 120

a maximum of two piece of data can be written in this preferred embodiment.

For example, according to a set associative system, a lot of writing can also be simultaneously performed by controlling a way by +CREATIVE_NEW, +UPDATE_OLD_ENTRY, +ERACE_ENTRY or another way selecting signal, etc.

Fig. 25 shows an example configuration of a reservation station in the case where writing in the reservation station is available after the completion of an instruction execution under IID (Instruction ID) control.

In Fig. 25, in addition to the configuration shown in Fig. 16, the reservation station 120 (120-2) is configured to register both a CSE-Valid flag, which is described later, and the IID of the instruction completion process unit 19. By doing this, a signal RSWx_CSE_VAL shown in Fig. 26 can be utilized, and whether an instruction is executed and completed can be judged.

A CSE-Valid flag is turned off by comparing the ID of an executed and completed instruction inputted from the instruction complete process unit 19 (COMMIT_BR_IID) with IID entries in the reservation station 120. If an instruction execution is

temporarily stopped due to an interruption, etc., the CSE-Valid flag is compulsorily turned off by a signal +FLUSH_RS. By doing this, an entry corresponding to an instruction for which the execution could not be completed due to an interruption, etc., does not remain.

If the CSE-Valid flag is ON, the execution of an instruction is not completed yet. Therefore, a signal obtained by suppressing a signal +RSW_x_VALID using this flag can be transmitted to a write selection circuit instead of +RSW_x_VALID shown in Fig. 18.

Fig. 26 shows an example configuration of the CSE valid circuit of a write reservation station.

The update valid signals of the branch history 20 of the respective entries RDW0-RSW3 of the No. 1 through No. 3 branch histories of the reservation station 120 (+BRHIS_UPDATE_VALID) are ON and the reservation station 120 is invalid (-RSW_x_VALID is ON) or if the reservation stations are full (+RSW_FULL is ON) and the reservation station 120 is selected (+SEL_RSW_x_WRITE), concerning the No. 0 branch history of the reservation station 120, a signal is inputted to the set ports of flip-flops 221-1 - 221-4, and a signal +RSW_x_CSE_VALID is outputted. The same process applies to the No. 1 through No. 3 of the reservation

station 120. However, in these cases, a priority circuit 223 is provided in mid-course. This priority circuit 223 is configured in such a way that priority decreases in ascending order of the number of reservation stations.

If COMMIT_BR_IID inputted from the instruction completion process management unit 19 in a cycle W and RSWx_IID recorded in the reservation station 120 are compared by comparators 222 (222-0 - 222-3) and if the signals match, the flip-flops 221-1 - 221-4 are reset. If a signal +FLUSH_RS outputted at the time of re-instruction fetch is inputted, the flip-flops 221-1 - 221-4 are also reset. Alternatively, if -RSWx_VALID, which is a signal obtained by logically inverting the output of the circuit shown in Fig. 24, is ON, the flip-flops 221-1 - 221-4 are reset.

If in a circuit shown in Fig. 26, a signal -RSWx_VALID is simultaneously inputted to OR circuits 224-0 - 224-3 and AND circuits 225-0 - 225-3, there is a possibility that a set signal and a reset signal may be simultaneously inputted. In this case, the circuit is configured in such a way that priority is given to the set signal.

Fig. 27 shows the data storage configuration of the write reservation station shown in Fig. 25.

If branch history information is inputted to a latch circuit 230 and +RSWx_VALID becomes ON, the branch history information is stored and outputted as RSWx_ branch history information.

5 Here, x corresponds to the digits 0 through 3, and the same number of the circuit shown in Fig. 27 as the entries of the reservation station 120, specifically, the number of entries of No. 1 through No. 3 branch histories of the reservation station 120 are provided.

10 Fig. 28 shows an example configuration of a CSE valid circuit in the case where a branch prediction unit is provided with a return address stack.

15 A return address stack is configured to operate if a completed branch instruction (to write history information) corresponds to a sub-routine call instruction or sub-routine return instruction.

20 When there is a temporary execution stoppage due to an interruption, etc. (a signal +RS1 is ON), it is sufficient if information indicating that the instruction corresponds to the sub-routine call or return of the branch history information which exists in the reservation station 120 is nullified instead of turning a Valid signal (the CSE-Valid flag of the reservation station 120) (see Fig. 25) off. It is

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Two portions including the flip-flops 241-1 and 241-2 located in the lower section are extracted to indicate that the portions are the sub-routine call instruction and sub-routine return instruction of the branch history information shown in Fig. 27.

If +RS1 is ON and +RSWx_CSE_VAL is also ON, the output of an AND circuit 244 becomes "0" and the flip-flops 241-1 and 241-2 are reset. If +RSWx_VALID, which is the output of the circuit shown in Fig. 24, is OFF and the instruction is a sub-routine call instruction, +BR_COMP_SUBROUTINE_CALL becomes ON and is inputted to the flip-flops 241-1 and 241-2. In this case, if the instruction is a sub-routine return instruction, +BR_COMP_SUBROUTINE RTN becomes ON and is inputted to

the flip-flops 241-1 and 241-2.

Specifically, if an instruction execution is not completed (+RSWx_CSE_VAL = 0) or there is no temporary execution stoppage due to an interruption, etc., (+RS1 = 0) and the entry of the reservation station 120 is valid (+RSWx_VALID = 1), an ON signal is inputted to the terminal IH of the flip-flops 241-1 and 241-2, and a signal indicating that the instruction is a sub-routine call instruction or a sub-routine return instruction is stored and outputted as +RSWx_SUBROUTINE_CALL or +RSWx_SUBROUTINE_RTN.

Fig. 29 shows an example circuit for nullifying the entry of the reservation station if an instruction execution is temporarily stopped due to an interruption, etc.

+SET_RSWx_VAL, which is a signal to be inputted to the set terminal of each of the flip-flops 211-1 - 211-4 shown in Fig. 24, is inputted to the set terminal of a set/reset flip-flop 251 and is outputted as +RSWX_VALID. If +RST_RSWx_VAL to be inputted as the reset signal shown in Fig. 24 is inputted or an execution is temporarily stopped due to an interruption, etc., (+RS1 = 1) and an instruction execution is not completed yet (+RSWx_CSE_VAL = 1), the set/reset flip-flop 251 is reset.

Fig. 30 shows one preferred embodiment of a bypass hit circuit.

An address comparison (branch prediction) unit 263 comprised of seven comparators 265 (265-1 - 265-7) varies depending on the nature of the branch prediction method of the branch history 20 and should be appropriately configured by a person having ordinary skill in the art. Therefore, only a brief description is made of the address comparison unit 263. Writing is bypassed and data in the write reservation station 120 and branch prediction unit (RSBRx in Fig. 30) can be designated as a search target by generating a branch destination address BRHIS_TIAR.

Specifically, the address comparison unit 263 compares an inputted address IF_EAG requested to be read with the branch history 20 (BRHIS-RAMs #0 and #1), the entries #RSW0-3 of the reservation station 120 and an instruction addresses IAR which are outputted from the branch prediction unit #RSBRx. If these respective compared signals match, the address comparison unit 263 outputs corresponding branch destination address TIAR from selection circuits 267-1 - 267-7. Then, one of these signals is selected by a selection circuit 268 and is outputted as the branch

destination address of the branch history (BRHIS_TIAR). If in the branch prediction unit, a branch destination address generated inside is valid and the branch prediction succeeds, the address comparison unit outputs a branch destination instruction address to the selection circuit 267-7.

By combining the configurations described above, the performance of the information processing apparatus can be improved.

Although in the preferred embodiments described above, a lowercase x is attached to the ends of symbols, like RSWx for example, in the case of a reservation station, this means that a lowercase x can take digits 0 through 3 and there are configurations and signals corresponding to the respective digits. In other cases, an x suffix means that there are the same number of configurations and signals corresponding to symbols with the suffix as the number indicated by the suffix, and represents the configurations and signals.

According to the present invention, in the execution of a branch instruction, an instruction fetch request can be processed with priority by delaying the timing of writing of an entry in a branch history, and the process delay can thereby be avoided.

writing in said branch prediction unit the branch history information about a branch instruction which has failed in a branch prediction, said control unit writes the branch history information in said branch prediction unit after several clock cycles (several states).

5. The device according to claim 1, wherein when writing in said branch prediction unit the branch history information about a branch instruction which has failed in a branch prediction, said control unit writes the branch history information in said branch prediction unit after a re-instruction fetch request by the branch instruction is executed and several clock cycles (several states) after the re-instruction fetch request is executed.

6. The device according to claim 1, wherein if the instruction execution processing apparatus is provided with a temporary instruction buffer unit temporarily storing an instruction string outputted from said memory unit,

said control unit writes the branch history information of the branch instruction in said branch prediction unit several clock cycles (several states)

after there is a write request of a branch instruction if the temporary instruction buffer unit is empty and there is no instruction fetch request.

5 7. The device according to claim 1, wherein if the instruction execution processing apparatus is provided with a temporary instruction buffer unit temporarily storing an instruction string outputted from said memory unit,

10 said control unit does not promptly write a branch history of a branch instruction to be requested to be written in said branch prediction unit, waits for a next instruction fetch request and writes the branch history information of the branch instruction
15 several clock cycles (several states) after the instruction fetch request is executed if the temporary instruction buffer unit is empty and there is not even one instruction fetch request.

20 8. The device according to any one of claims 4 through 7, wherein said control unit uses a counter to count the several clock cycles (several states).

25 9. The device according to claim 1, wherein when writing the branch history information of the branch

instruction which has failed in the branch prediction,
said control unit writes the branch history
information after an instruction decoding unit or said
temporary instruction buffer unit in the instruction
5 execution processing apparatus receives a fetch
instruction string corresponding to a re-instruction
fetch requested by the branch instruction.

10. The device according to claim 1, further
10 comprising:

a write reservation station unit temporarily
storing the branch history information to be written.

11. The device according to claim 10, wherein said
15 control unit registers in the reservation station unit
only the branch history information concerning a
branch instruction which must be written in said
branch prediction unit.

20 12. The device according to claim 11, wherein the
branch history information is about at least one of
a new entry registration, an entry content change or
an entry erasure.

25 13. The device according to claim 10, wherein if said

write reservation station unit is full and there is a request for registering in the write reservation station unit, said control unit writes in said branch prediction unit at least one group of branch history information, writing of which in the write reservation station unit is held and the branch history information of which has been requested to be registered.

10 14. The device according to claim 10, wherein if said branch prediction unit is configured to simultaneously write a plurality of entries and said write reservation station unit stores a plurality of valid information, writing of which is held, said control
15 unit simultaneously writes the plurality of information in a timing such that writing in said branch prediction unit is possible.

20 15. The device according to claim 1 or 10, wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, etc., which exits before a branch instruction, there is another branch instruction before the branch instruction when a branch
25 destination address is confirmed, and even if the

branch instruction cannot be completed, said control unit writes the branch history information of the branch instruction in said branch prediction unit or registers the information in the write reservation station unit.

16. The device according to claim 15, wherein said control unit provides a flag indicating that the branch history information is written or registered in the write reservation station unit for each corresponding branch instruction being processed.

17. A branch history information write control device in an instruction execution processing apparatus provided with a branch prediction unit performing a branch prediction of a branch instruction, comprising:

a return address stack unit; and
a control unit writing branch history information in the branch prediction unit, but controlling in such a way not to operate the return address stack if the branch instruction corresponds to a sub-routine call or return and the branch instruction is not executed although a write request of the branch history information of the branch instruction is issued to the branch prediction unit.

18. The device according to claim 10, wherein said control unit writes the branch history information, writing of which in the write reservation station unit is held when an execution of an instruction is completed.

19. The device according to claim 10, wherein said control unit writes branch history information of a corresponding entry in said branch prediction unit or said write reservation station unit when an execution of an instruction is completed.

20. The device according to claim 10, wherein if the instruction execution processing apparatus is provided with a unit controlling an execution completion of an instruction in its instruction control unit,

said control unit stores an ID assigned for each instruction, which is stored in the execution completion management unit, in an entry of the write reservation station unit.

21. The device according to claim 10, wherein if it is confirmed that a branch instruction corresponding to a valid entry of the write reservation station unit is neither executed nor completed due to an occurrence

of interruption, etc., the entry corresponding to the write reservation station unit is nullified.

22. The device according to claim 1, further comprising:

a bypass unit making branch history information, writing of which in said branch prediction unit is held, a research target of a branch prediction.

23. The device according to claim 10, further comprising:

a bypass unit making branch history information of a branch instruction which is being executed in its branch execution unit including the write reservation station unit, a research target of a branch prediction.

24. The device according to claim 23, wherein said bypass unit makes the branch history information a search target of a branch prediction when a conditional code for the branch instruction is confirmed if it is confirmed that the branch instruction is not branched and when a branch destination address is confirmed if it is confirmed that the branch instruction is branched.

25. The device according to claim 1, wherein a dual-port RAM in which writing and reading can be simultaneously executed independently is used for said branch prediction unit to hold an entry.

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26. An instruction control method in an apparatus provided with both a memory storing an instruction string, etc., and a branch prediction unit performing a branch prediction of a branch instruction, comprising:

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controlling in such a way that writing of branch history information in said branch prediction unit and control over the memory do not occur simultaneously.

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27. The method according to claim 26, wherein the branch history information is written in said branch prediction unit in a timing such that said memory cannot accept an instruction fetch request.

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28. The method according to claim 26, wherein the branch history information is written in said branch prediction unit in a timing of requesting a pre-fetch of an instruction.

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29. The method according to claim 26, wherein if the

branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written in said branch prediction unit
5 after several clock cycles (several states).

30. The method according to claim 26, wherein if the branch history information of a branch instruction which has failed in a branch prediction is written in
10 said branch prediction unit, the branch history information is written in said branch prediction unit after a re-instruction fetch request by the branch instruction is executed and several clock cycles (several states) after the re-instruction fetch
15 request is executed.

31. The method according to claim 26, further comprising:

temporary instruction buffer step temporarily
20 storing an instruction string, etc., outputted by said memory,

wherein if there is no instruction string to be stored in the temporary instruction buffer step and there is no instruction fetch request, the branch history
25 information of a branch instruction to be requested

to be written is written in said branch prediction unit several clock cycles (several states) after a write request is issued.

- 5 32. The method according to claim 26, further comprising:

temporary instruction buffer step temporarily storing an instruction string, etc., outputted by said memory,

- 10 wherein if there is no instruction string to be stored in the temporary instruction buffer step and there is no instruction fetch request, the branch history information of a branch instruction to be requested to be written is not promptly written in said branch
15 prediction unit, waits for a next instruction fetch request and is written several clock cycles (several states) after the instruction fetch request is executed.

- 20 33. The method according to claim 26, wherein when the branch history information of a branch instruction which has failed in a branch prediction is written in said branch prediction unit, the branch history information is written after its instruction decoding
25 unit or said temporary instruction buffer receives a

fetch instruction string corresponding to a re-instruction fetch requested by the branch instruction.

34. The method according to claim 26, further comprising:

write reservation station step temporarily storing the branch history information to be written.

35. The method according to claim 34, wherein only the branch history information concerning a branch instruction which must be written in said branch prediction unit is registered in said write reservation station step.

36. The method according to claim 35, wherein the branch history information is a new entry registration, an entry content change or an entry erasure.

37. The method according to claim 34, wherein if a storage capacity in the write reservation station step is full and further there is a register request on a branch instruction, branch history information of which must be written in the write reservation station step, at least one group of a branch history

information, writing of which is held in the write reservation station step and the branch history information which has been requested to be registered, is written.

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38. The method according to claim 34, wherein if said branch prediction unit is configured to simultaneously write a plurality of entries and the write reservation station unit stores a plurality of valid information, writing of which is held, a plurality of writing executions are performed in a timing such that writing in said branch prediction unit is available.

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39. The method according to claim 26 or 34, wherein if an instruction is conditionally encoded or branched by an execution completion of an execution instruction, etc., which exists before a branch instruction, there is another branch instruction before the branch instruction when a branch destination address is confirmed and even if the branch instruction cannot be completed, the branch history information of the branch instruction is written in said branch prediction unit or registered in the reservation station step.

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40. The method according to claim 39, wherein a flag indicating that the branch history information is written or registered in said write reservation station step is provided for each corresponding branch instruction being processed.

41. An instruction control method in an apparatus provided with both a branch prediction unit performing a branch prediction of a branch instruction and a return address stack, comprising:

controlling in such a way to write branch history information in said branch prediction unit, but not to operate the return address stack if a branch instruction has not been executed although a request for writing of the branch history information in the branch prediction unit is issued by an instruction corresponding to a sub-routine call or return obtained as an execution result of the branch instruction.

42. The method according to claim 34, wherein branch history information, writing of which is held in said write reservation station step, is written when an execution of an instruction is completed.

43. The method according to claim 34, wherein branch

history information of a corresponding entry is written in said write reservation station unit when an execution of an instruction is completed.

5 44. The method according to claim 34, wherein an instruction control unit further comprises the step of managing an execution completion of an instruction, and stores an ID assigned for each instruction which is stored in said execution completion management
10 step, in an entry in said write reservation station step.

45. The method according to claim 34, wherein if it is found that a branch instruction corresponding to
15 a valid entry stored in said write reservation station step due to an occurrence of interruption, etc., is not executed and completed, a corresponding entry stored in said write reservation station step is nullified.

20 46. The method according to claim 26, wherein branch history information, writing of which in said branch prediction unit is held, is a search target of a branch prediction.

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Abstract of the Disclosure

If a re-instruction fetch request is inputted to a box 30, a signal for holding writing in a branch history or a signal for holding a re-instruction fetch is generated. A signal for holding the re-instruction fetch, branch history information, a branch instruction address and a branch destination instruction address are inputted to the box 31. The box 31 outputs these data, and simultaneously generates a new entry in the branch history, updates an old entry or generates a signal for instructing to erase an entry. These data are inputted to the box 32, and a signal for instructing whether to write a branch instruction address, a branch destination instruction address or branch history information are generated.

BRANCH HISTORY WRITING

↓

BC	U	W							
NOP1	IA	IT	IB	IR	D				
NOP2					D				
NOP3					D				
NOP4							D		
NOP5		←→	IA	IT	IB	IR	D		
NOP6		↑						D	
NOP7								D	
NOP8									D

1 CLOCK WAITING

FIG. 1 Prior Art

EXAMPLE OF SHORT LOOP

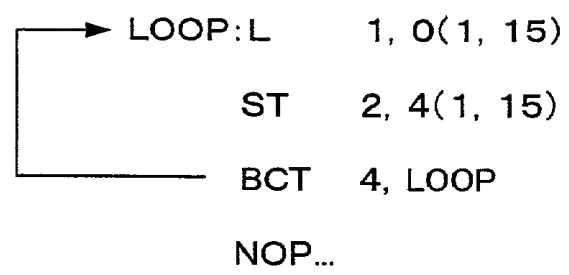


FIG. 2A Prior Art

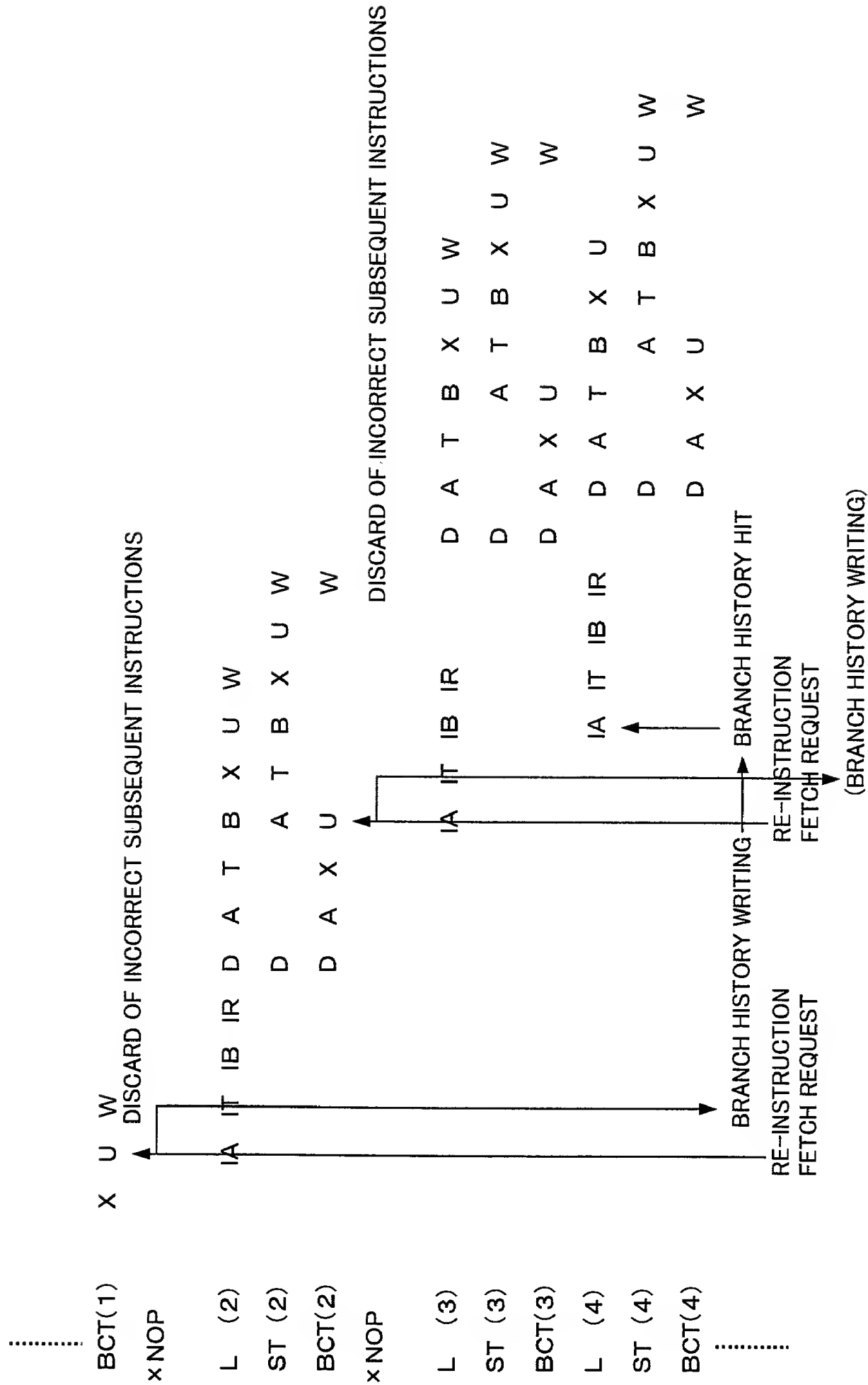
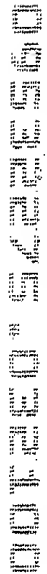


FIG. 2B Prior Art

BC	U	W					
NOP1	IA	IT	IB	IR	D		
NOP2					D		
NOP3					D		
NOP4							D
NOP5		IA	IT	IB	IR	D	
NOP6						D	
NOP7							D
NOP8							D

F I G. 3

[illegible][illegible]

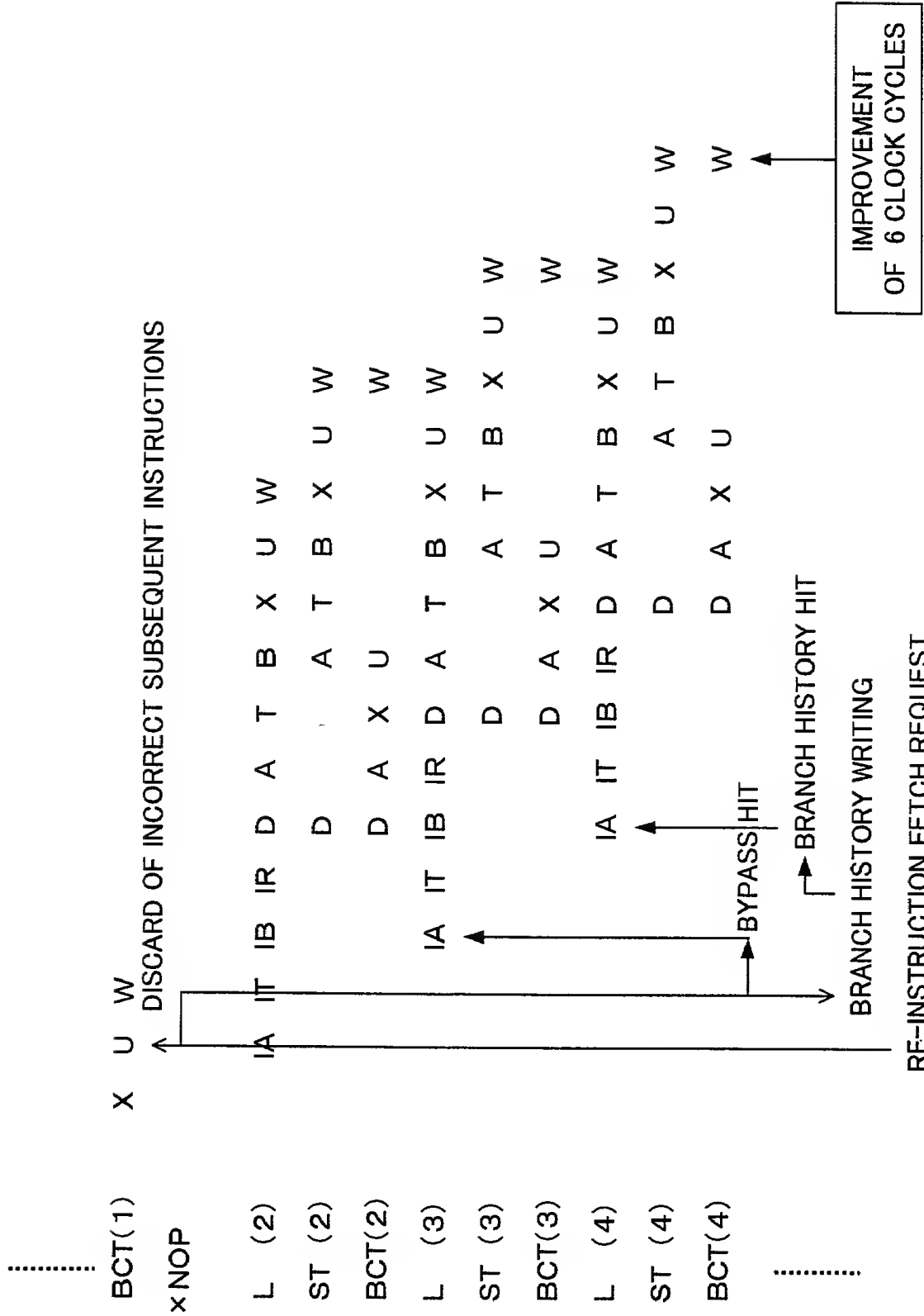


FIG. 4B

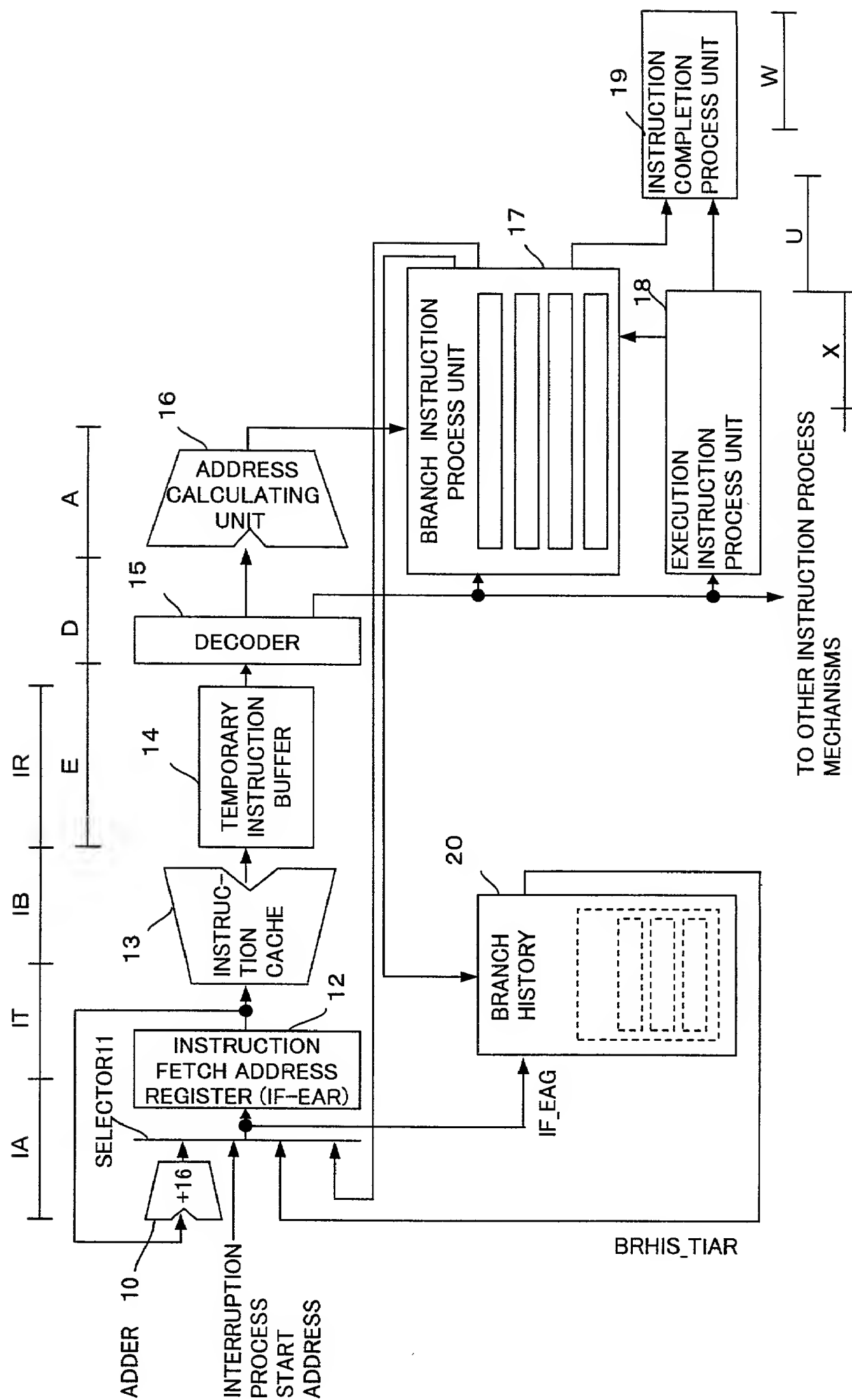


FIG. 5

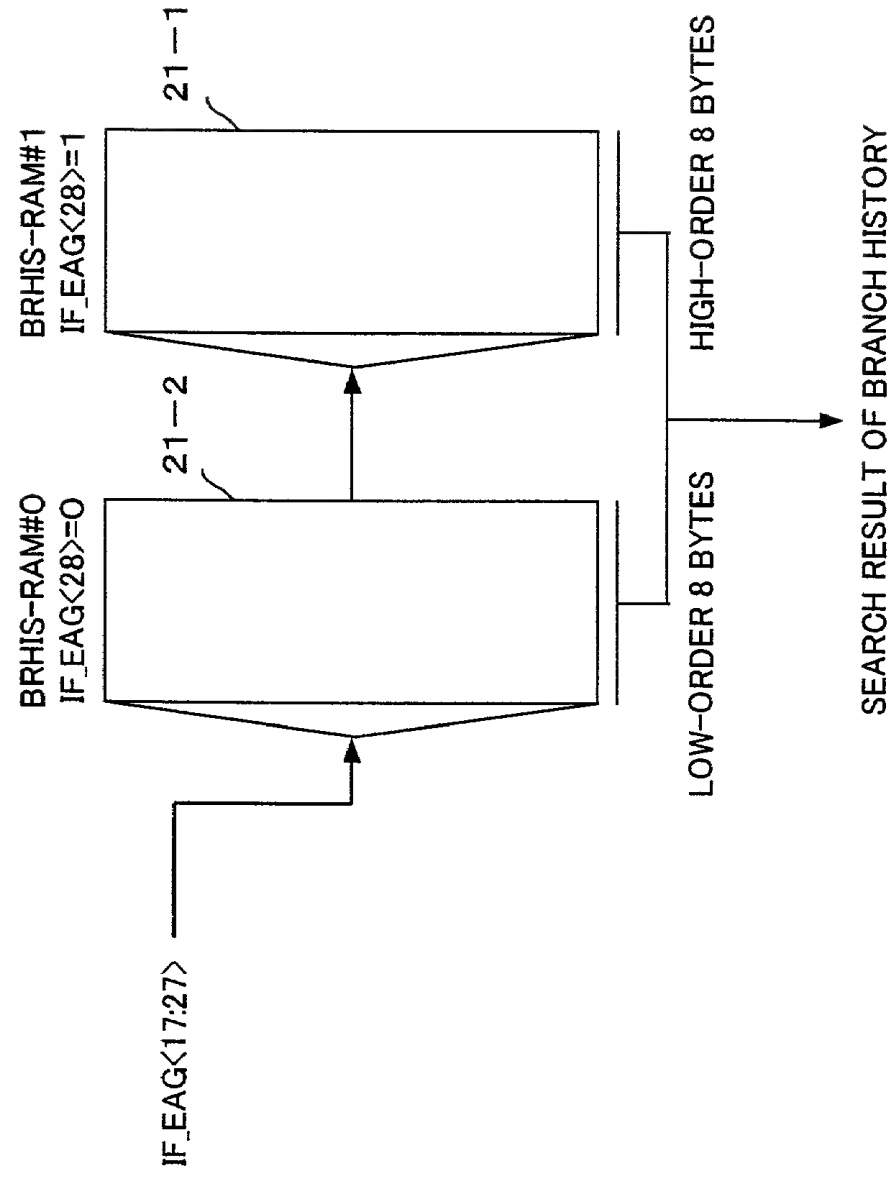


FIG. 6

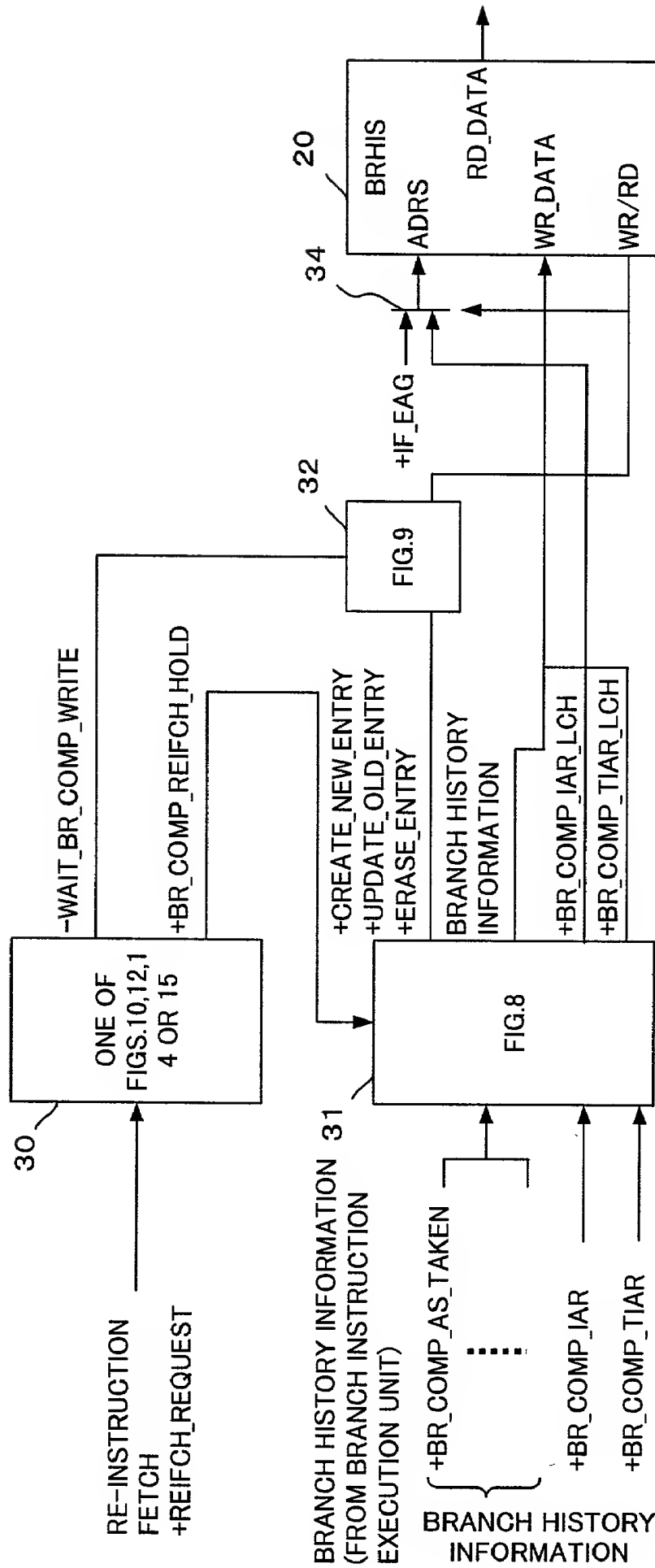


FIG. 7

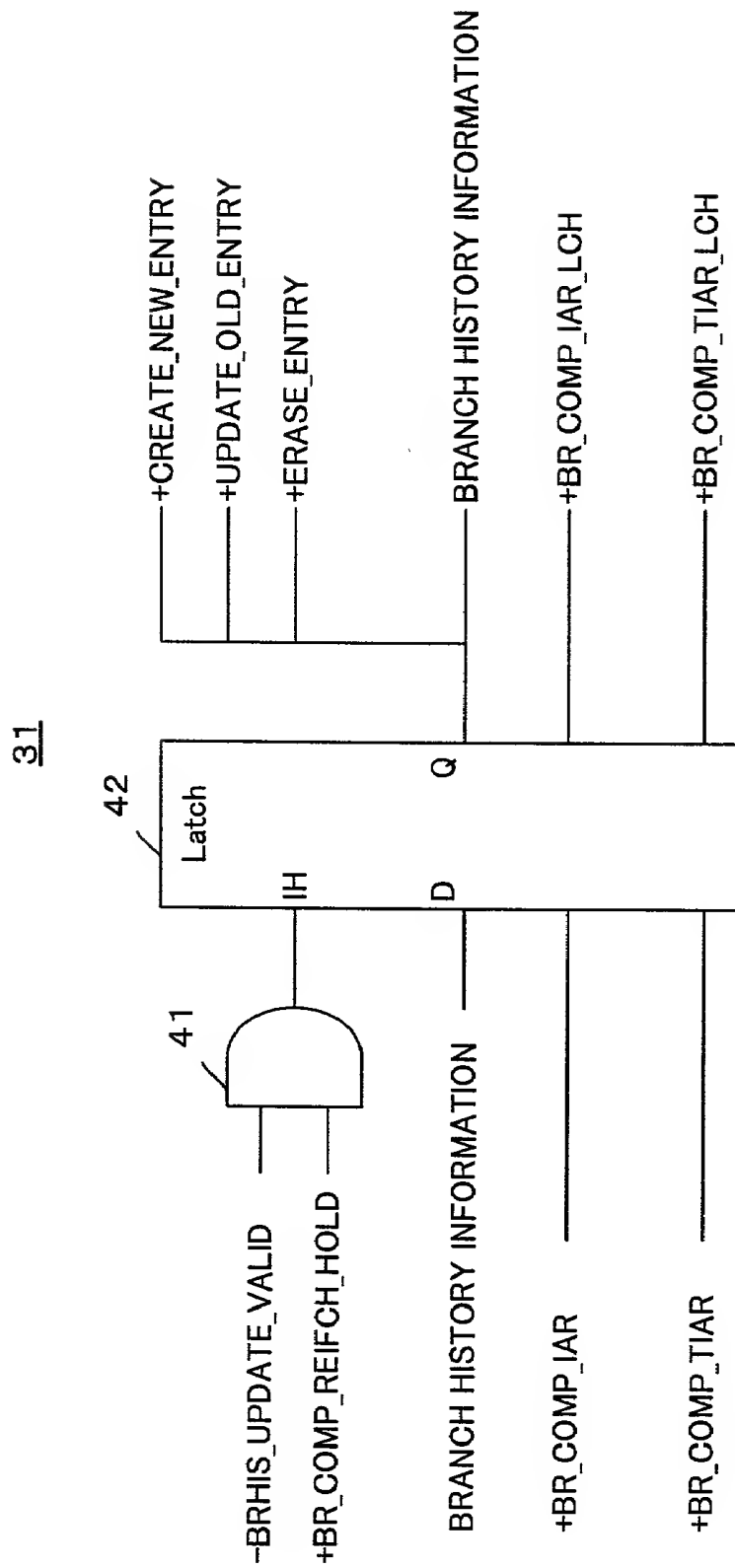


FIG. 8

32

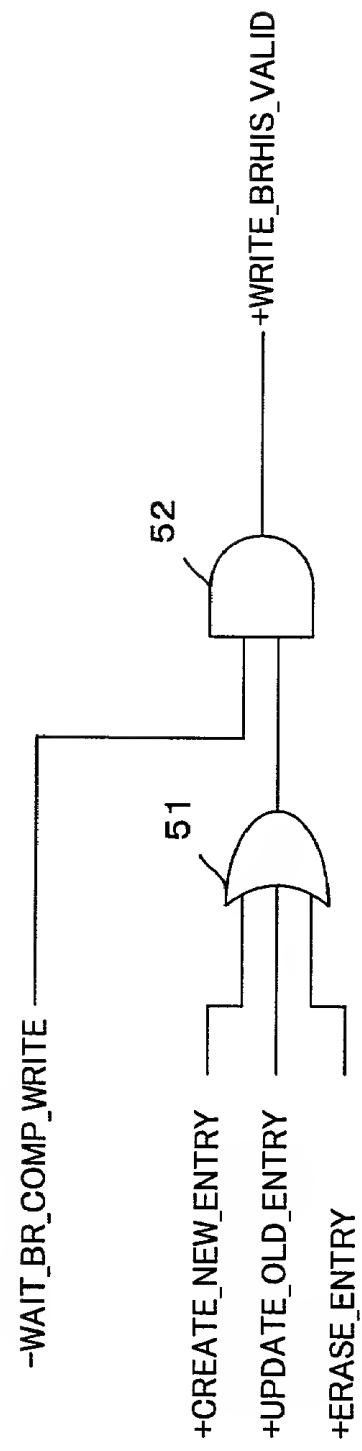


FIG. 9

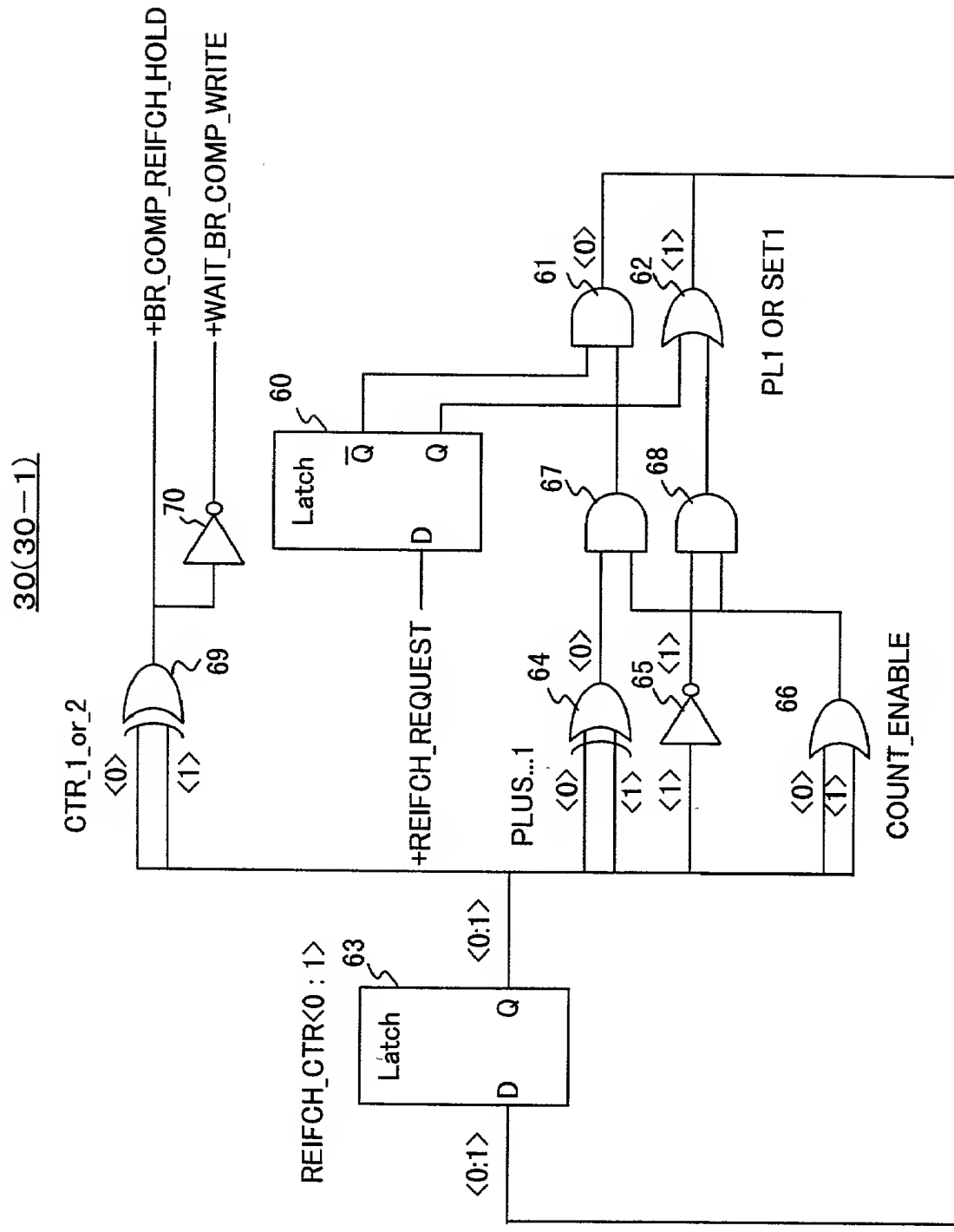


FIG. 10

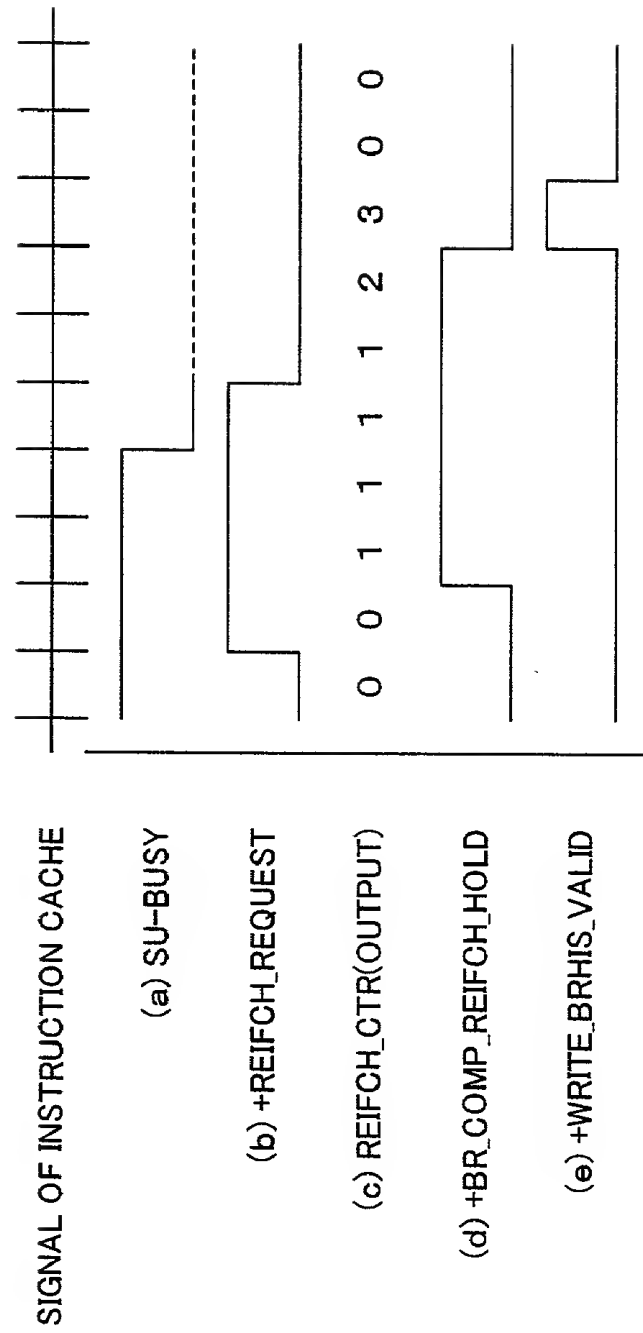


FIG. 11

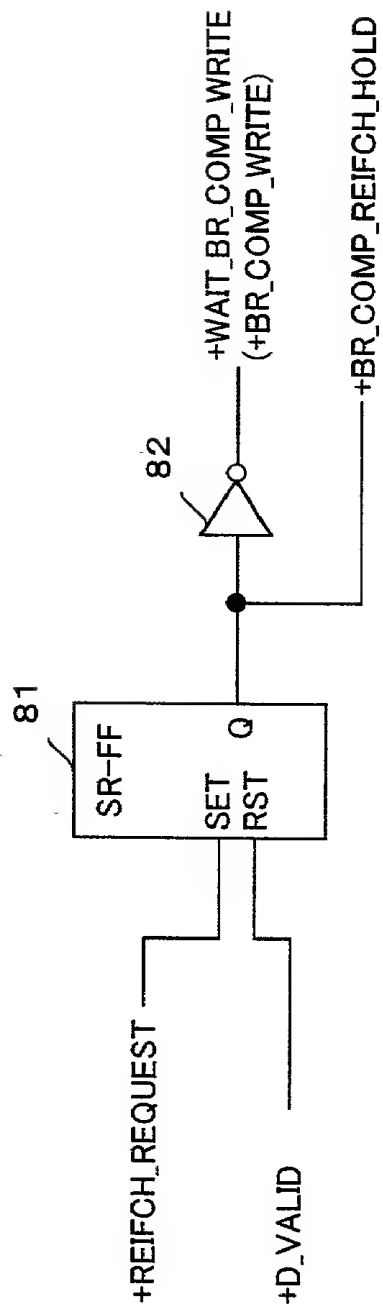


FIG. 12

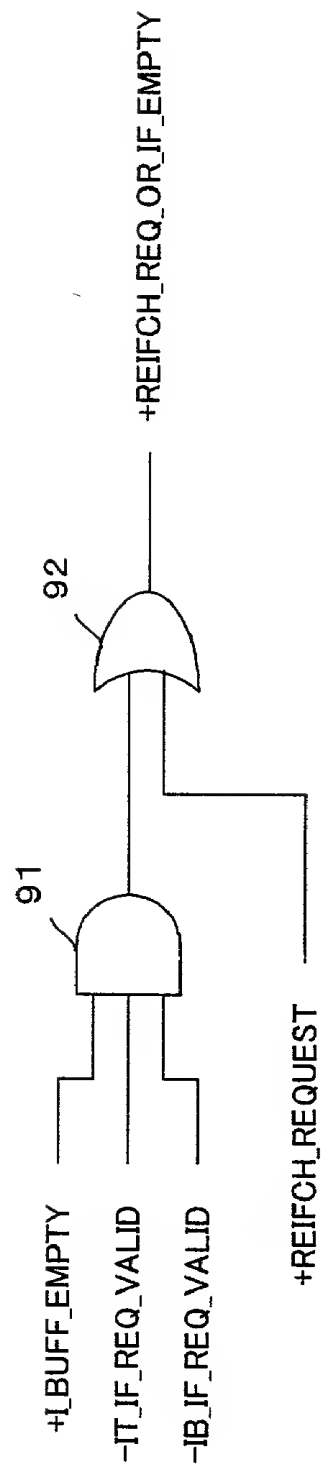


FIG. 13

30(30-4)

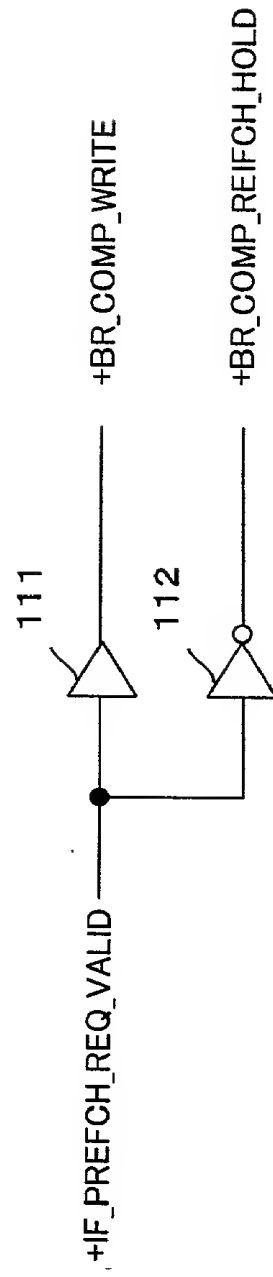


FIG. 15

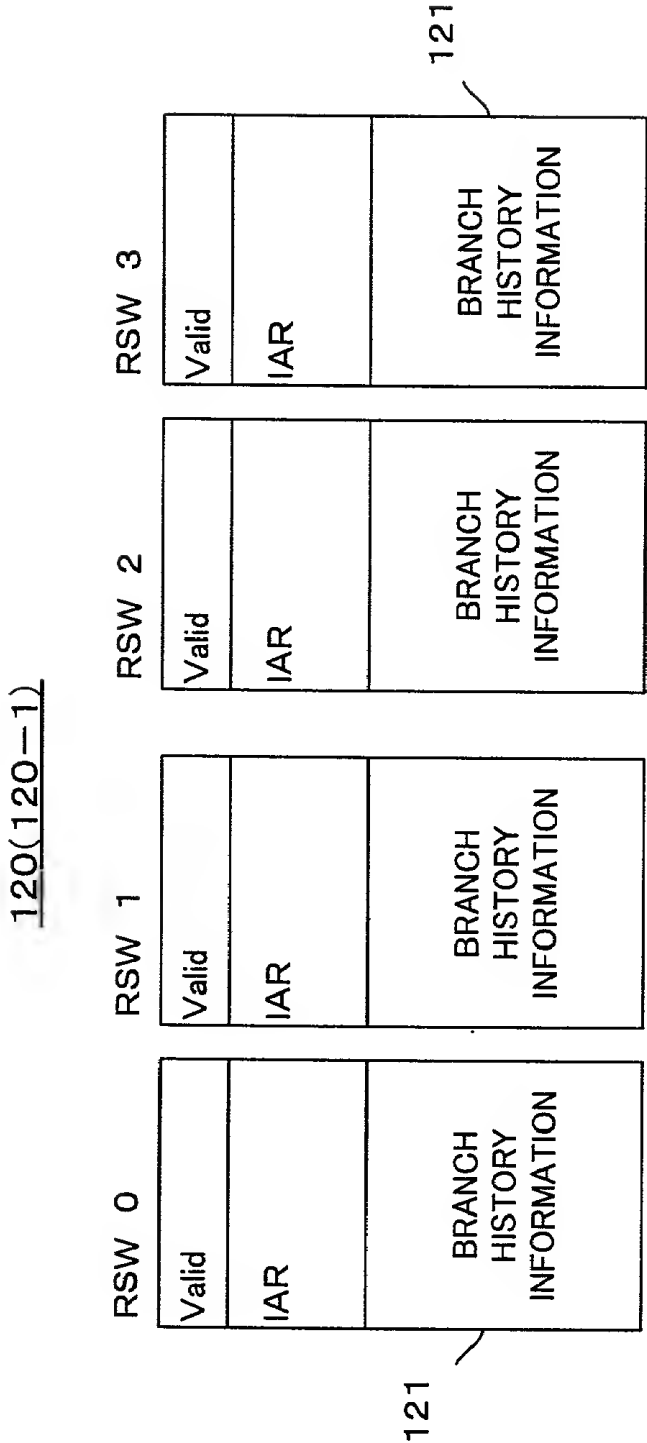


FIG. 16

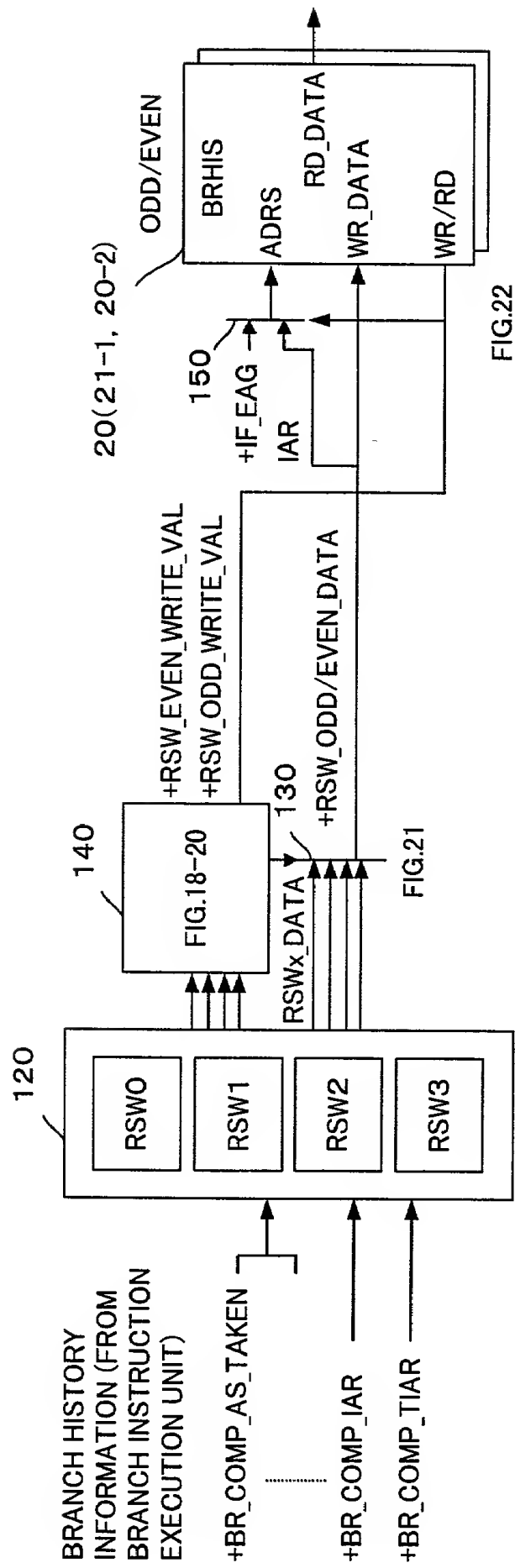


FIG. 17

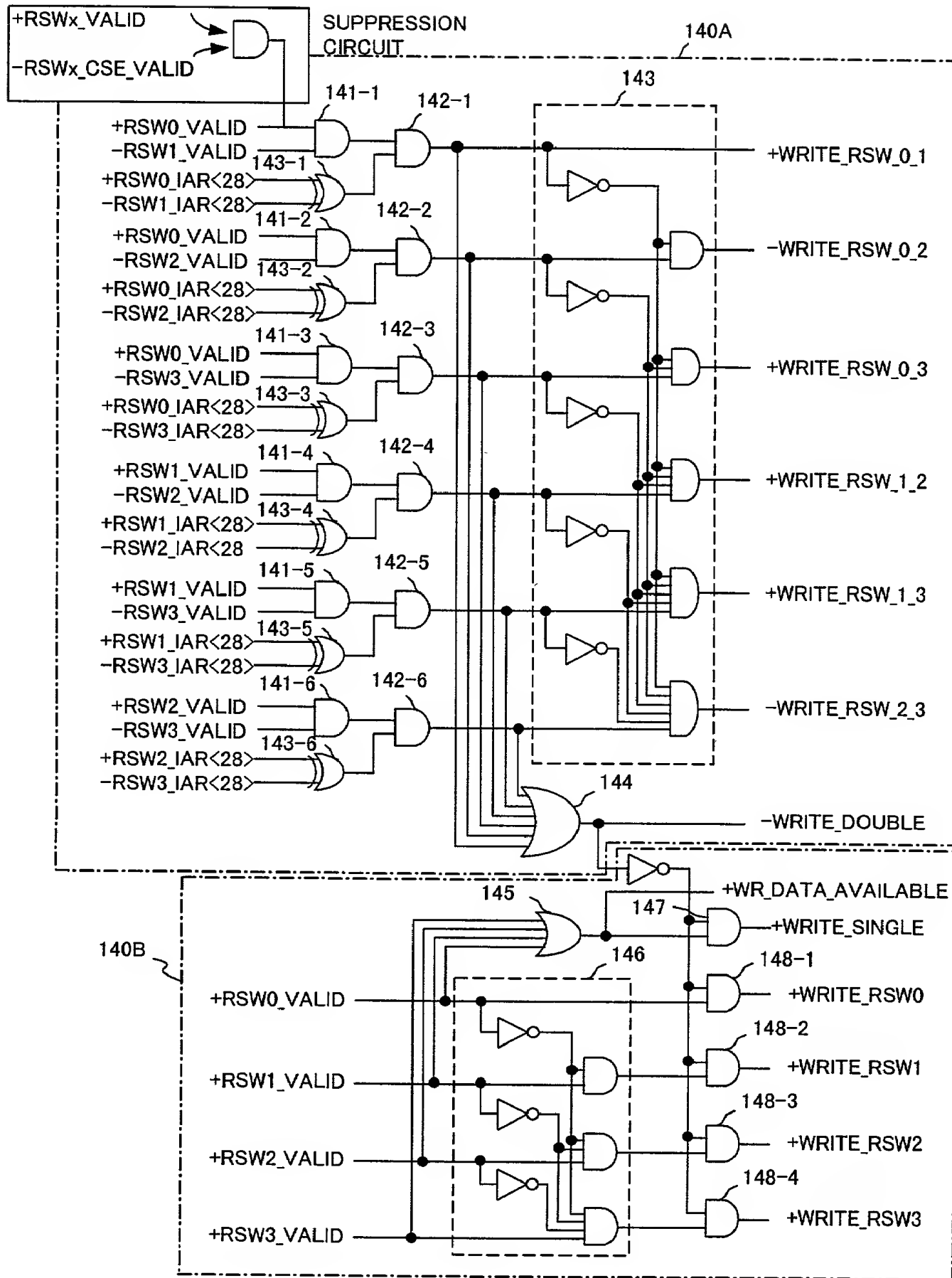


FIG. 18

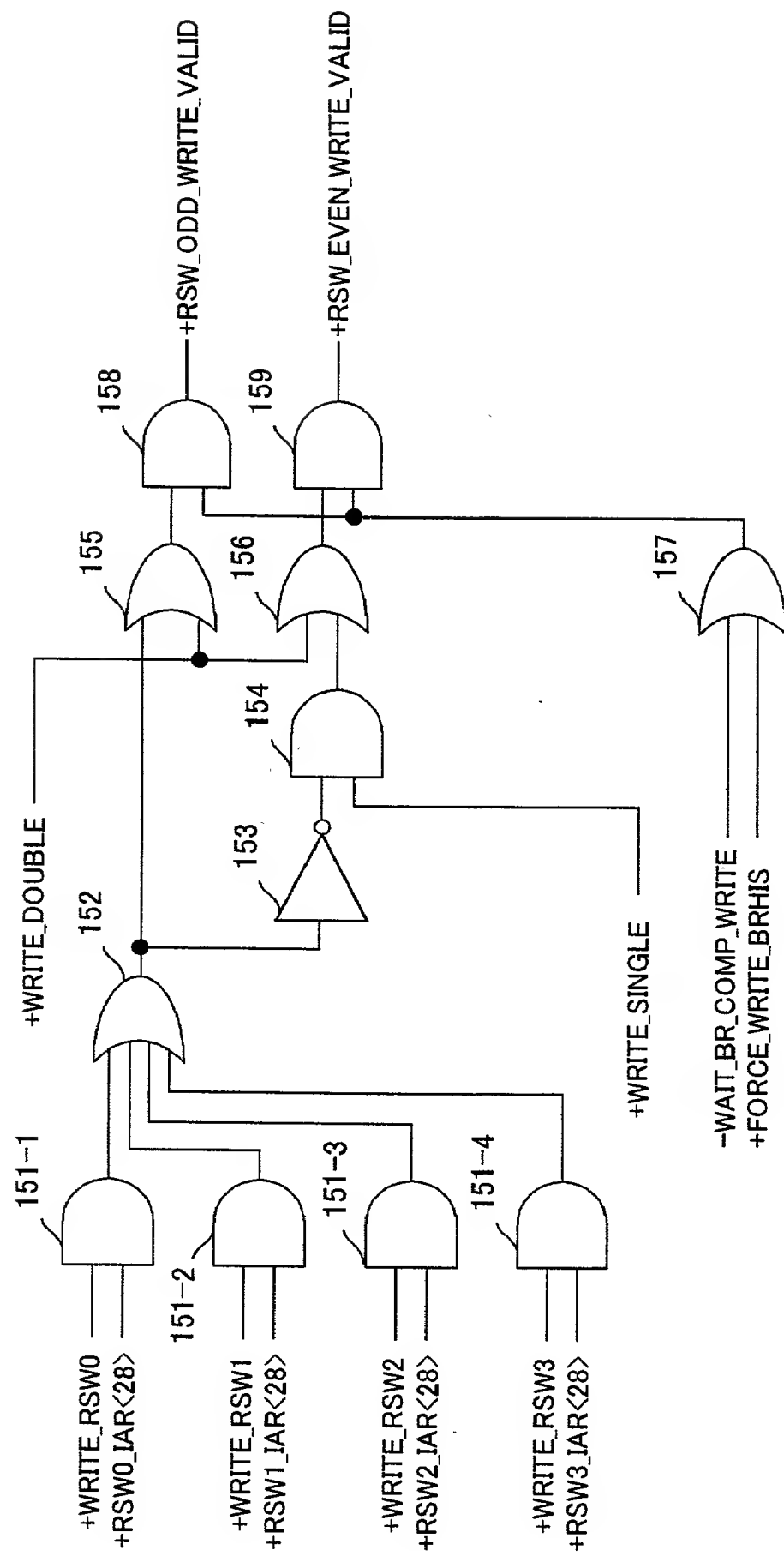


FIG. 19

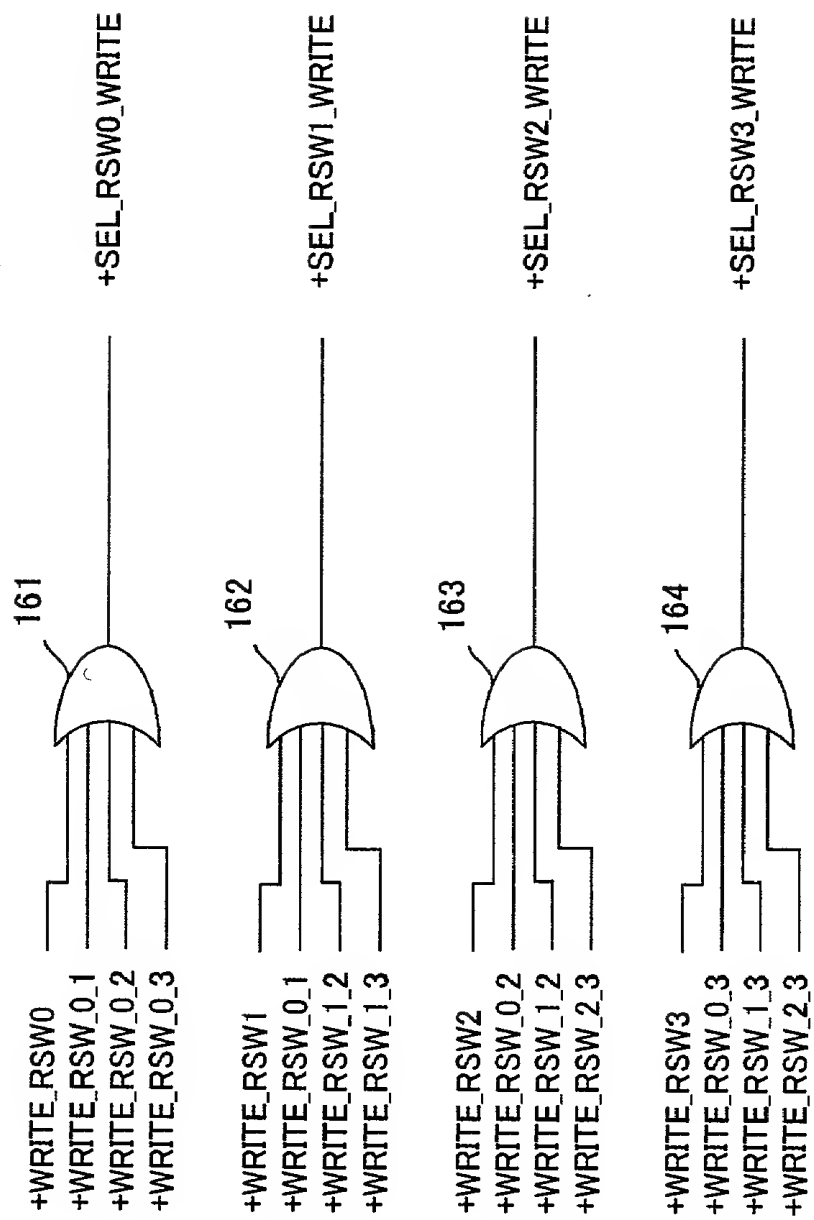


FIG. 20

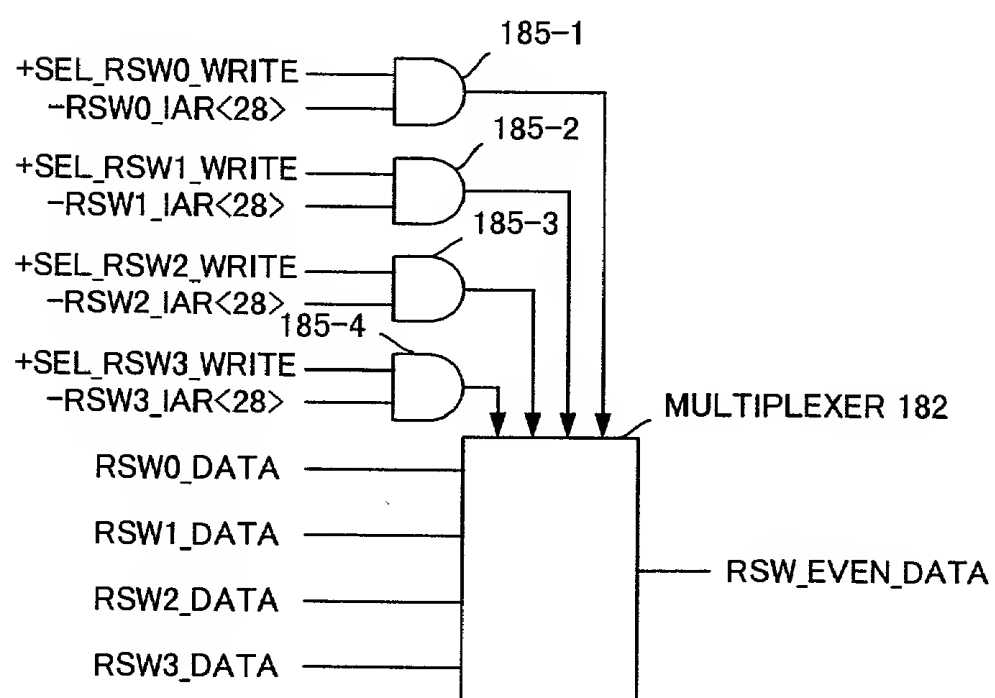
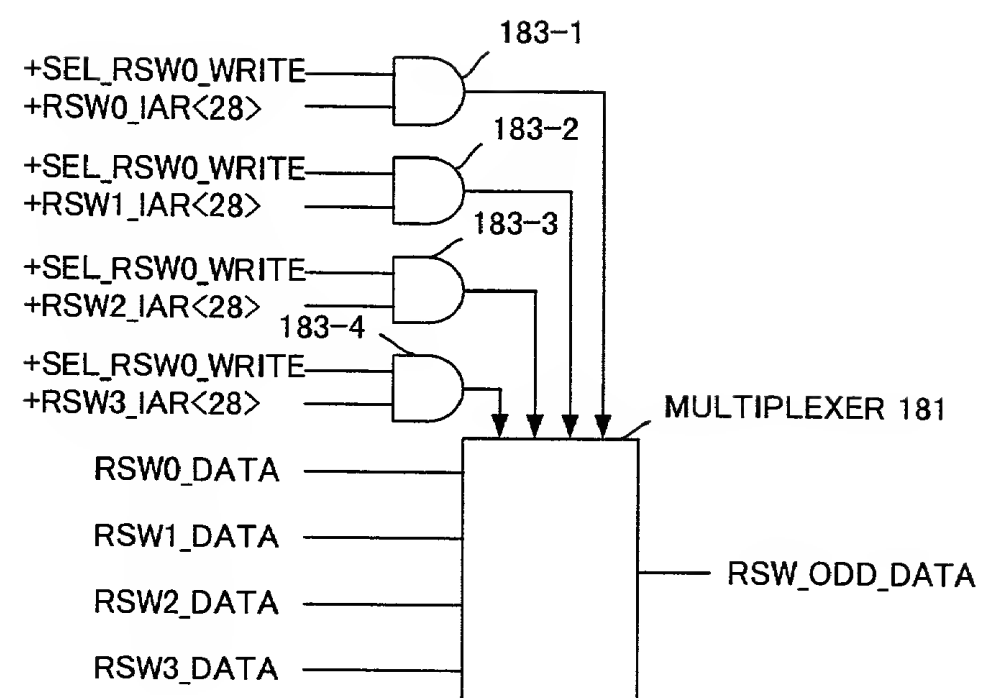
[illegible]

FIG. 21

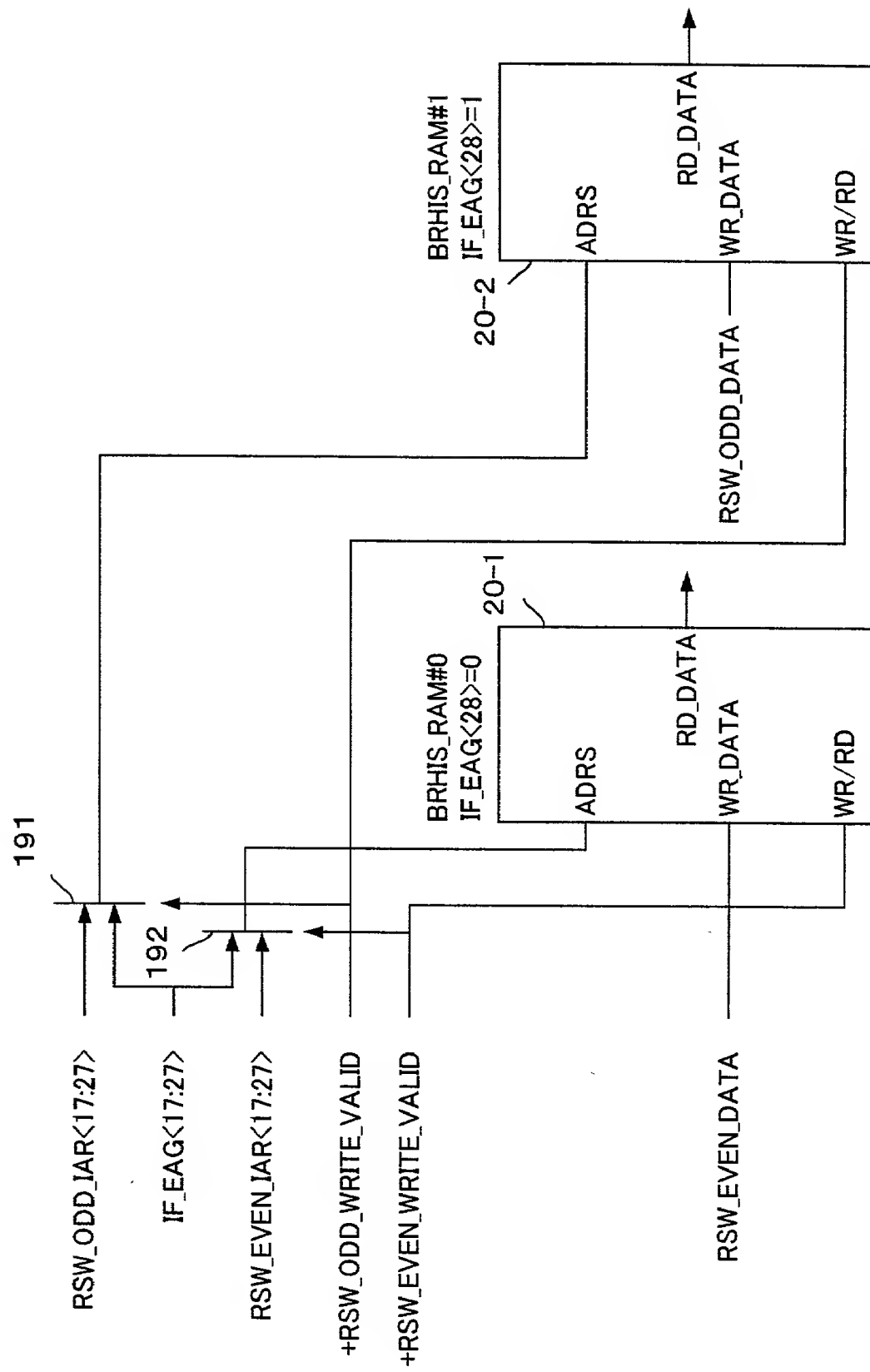


FIG. 22

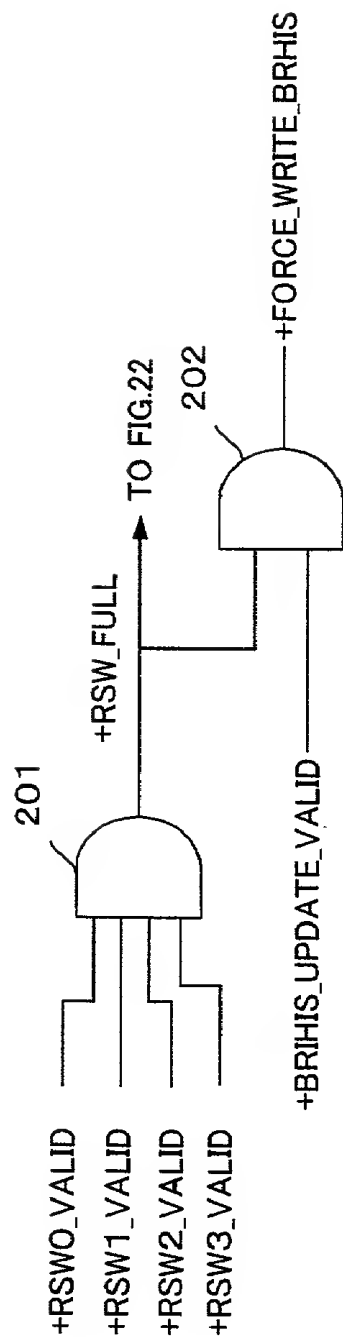


FIG. 23

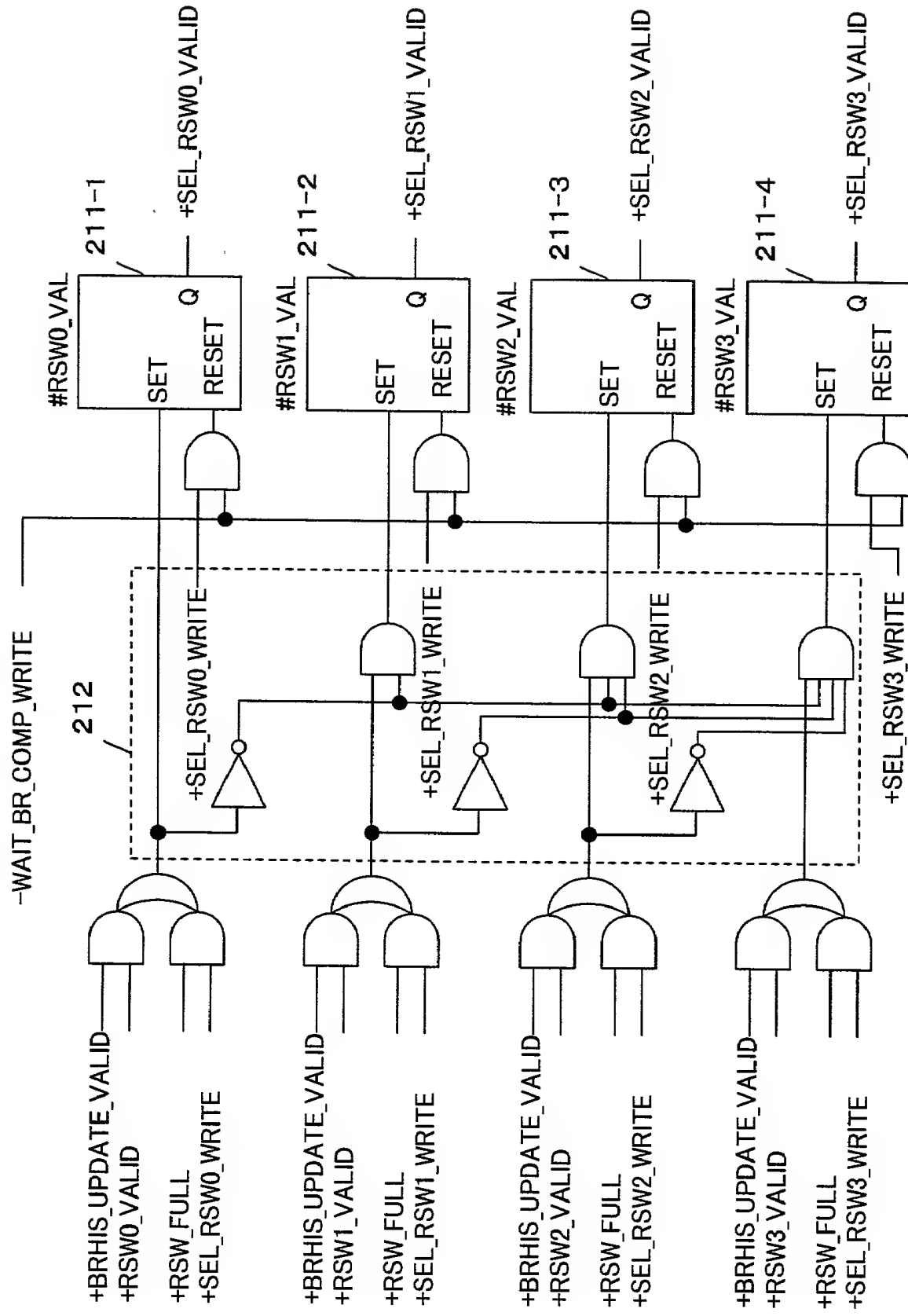


FIG. 24

120(120-2)

RSW 0	RSW 1	RSW 2	RSW 3
Valid	Valid	Valid	Valid
IAR	IAR	IAR	IAR
CSE-Valid	CSE-Valid	CSE-Valid	CSE-Valid
IID	IID	IID	IID
BRANCH HISTORY INFORMATION	BRANCH HISTORY INFORMATION	BRANCH HISTORY INFORMATION	BRANCH HISTORY INFORMATION

FIG. 25

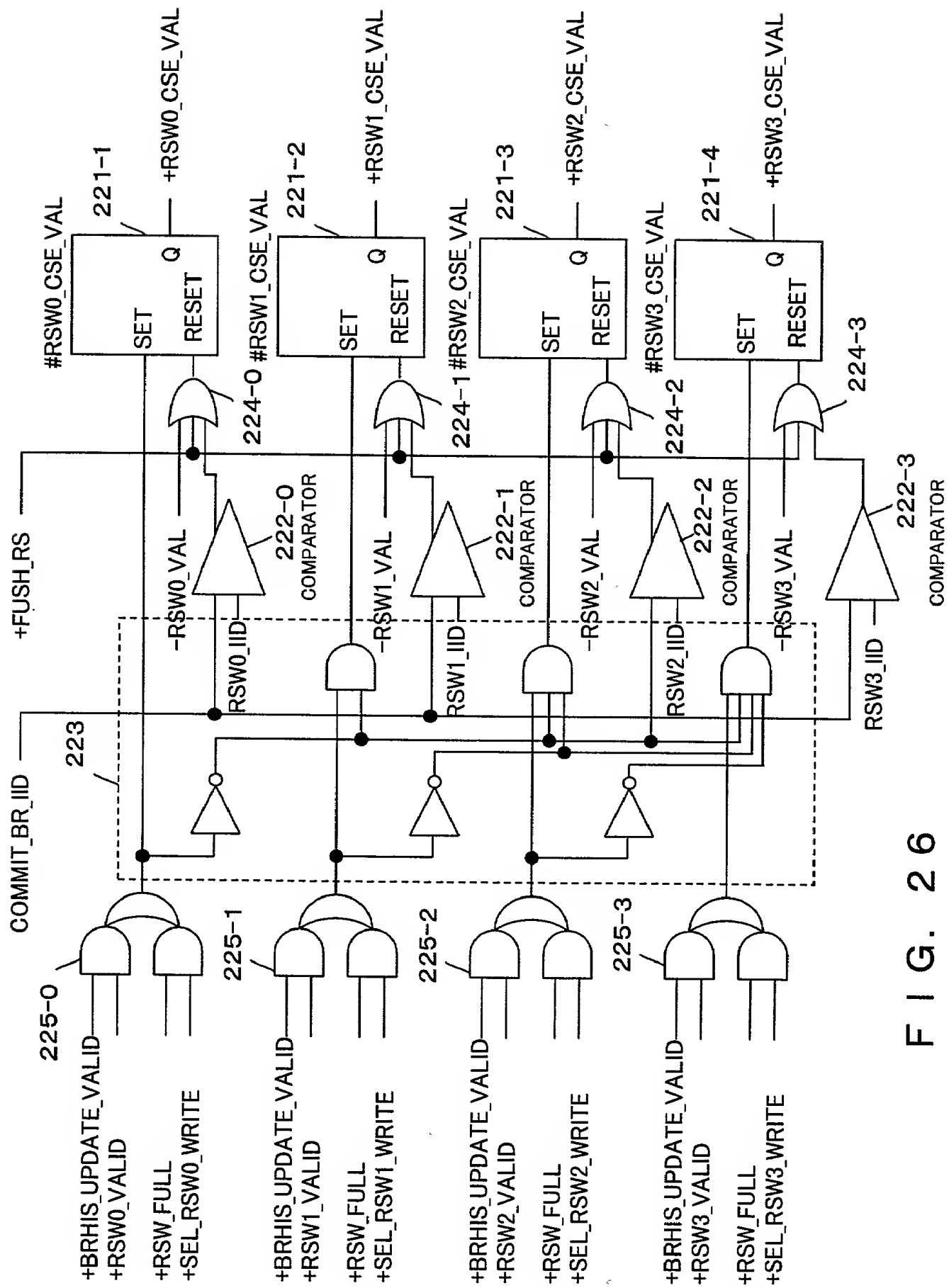


FIG. 26

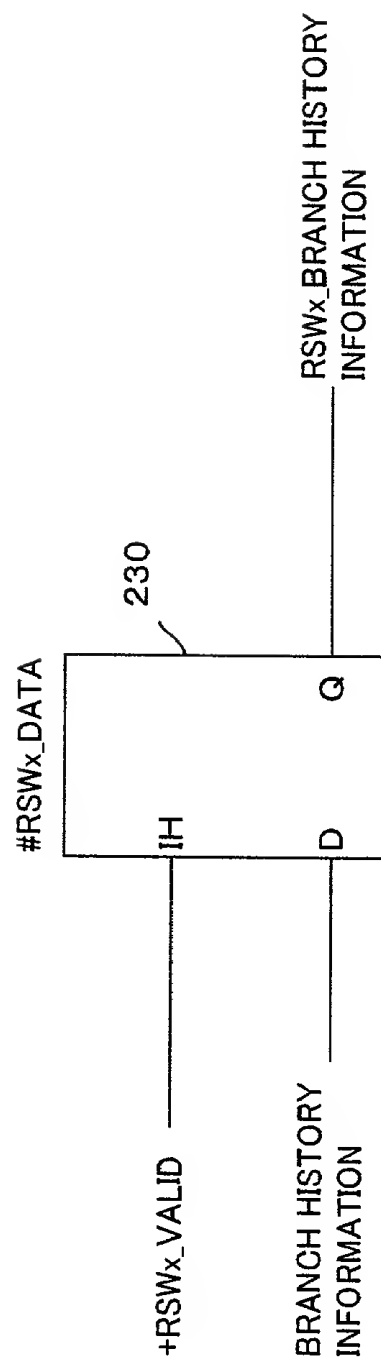


FIG. 27

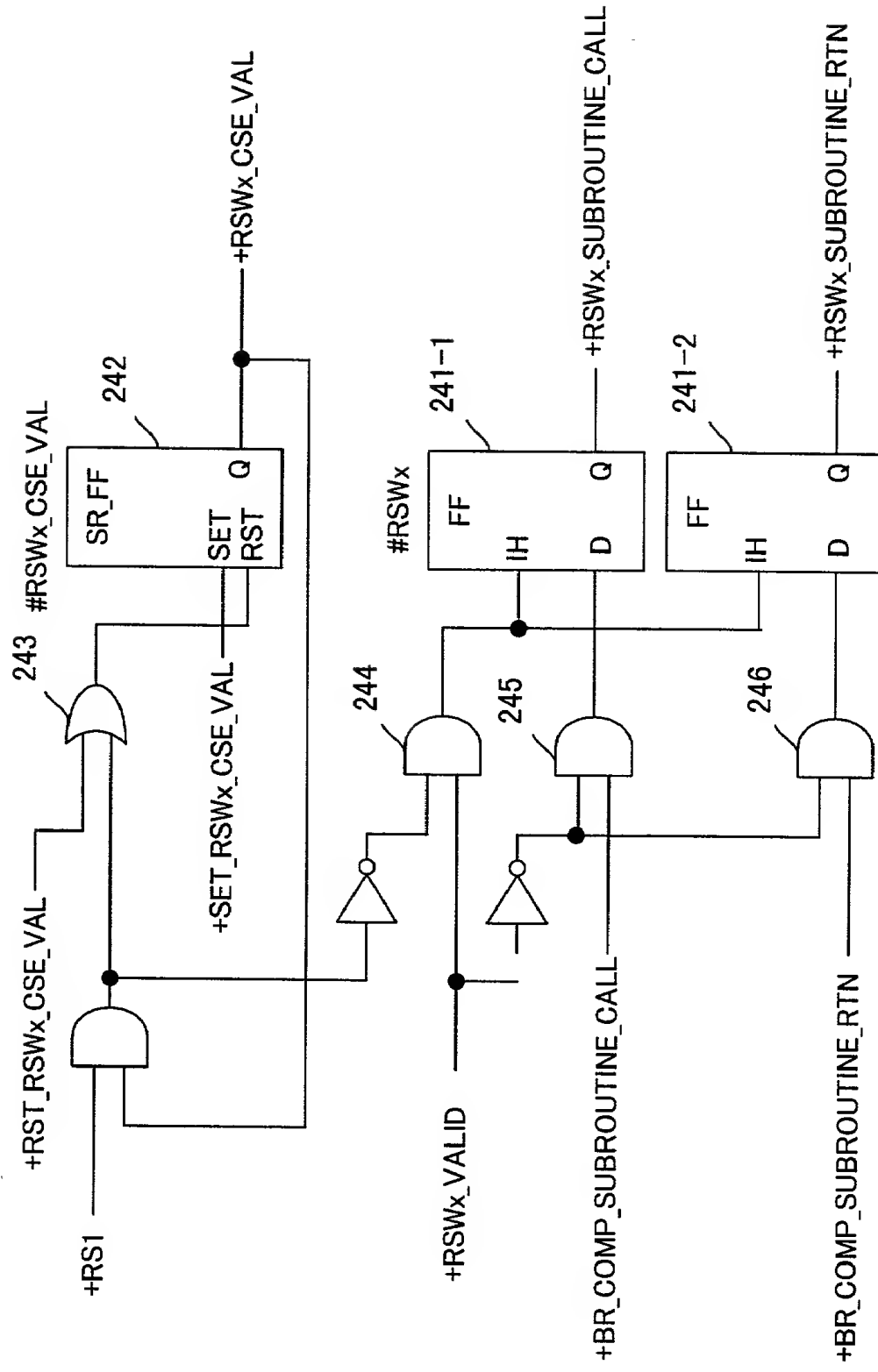


FIG. 28

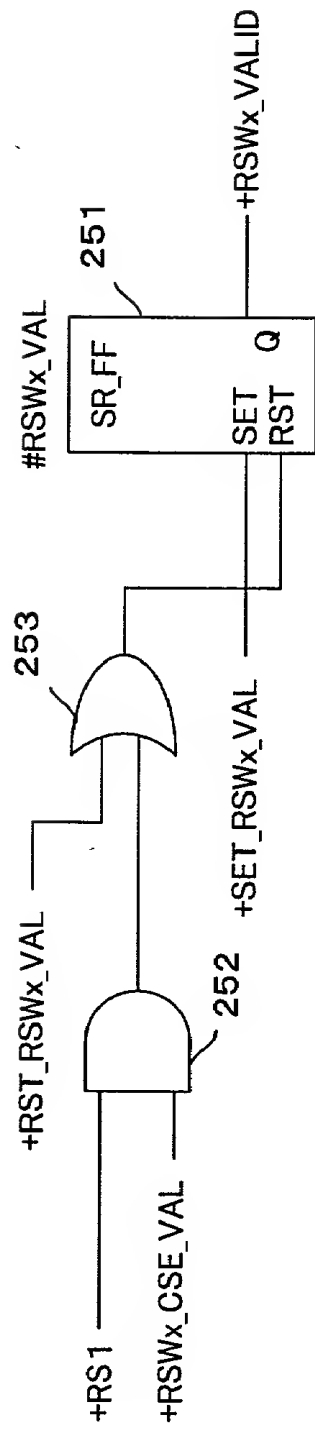
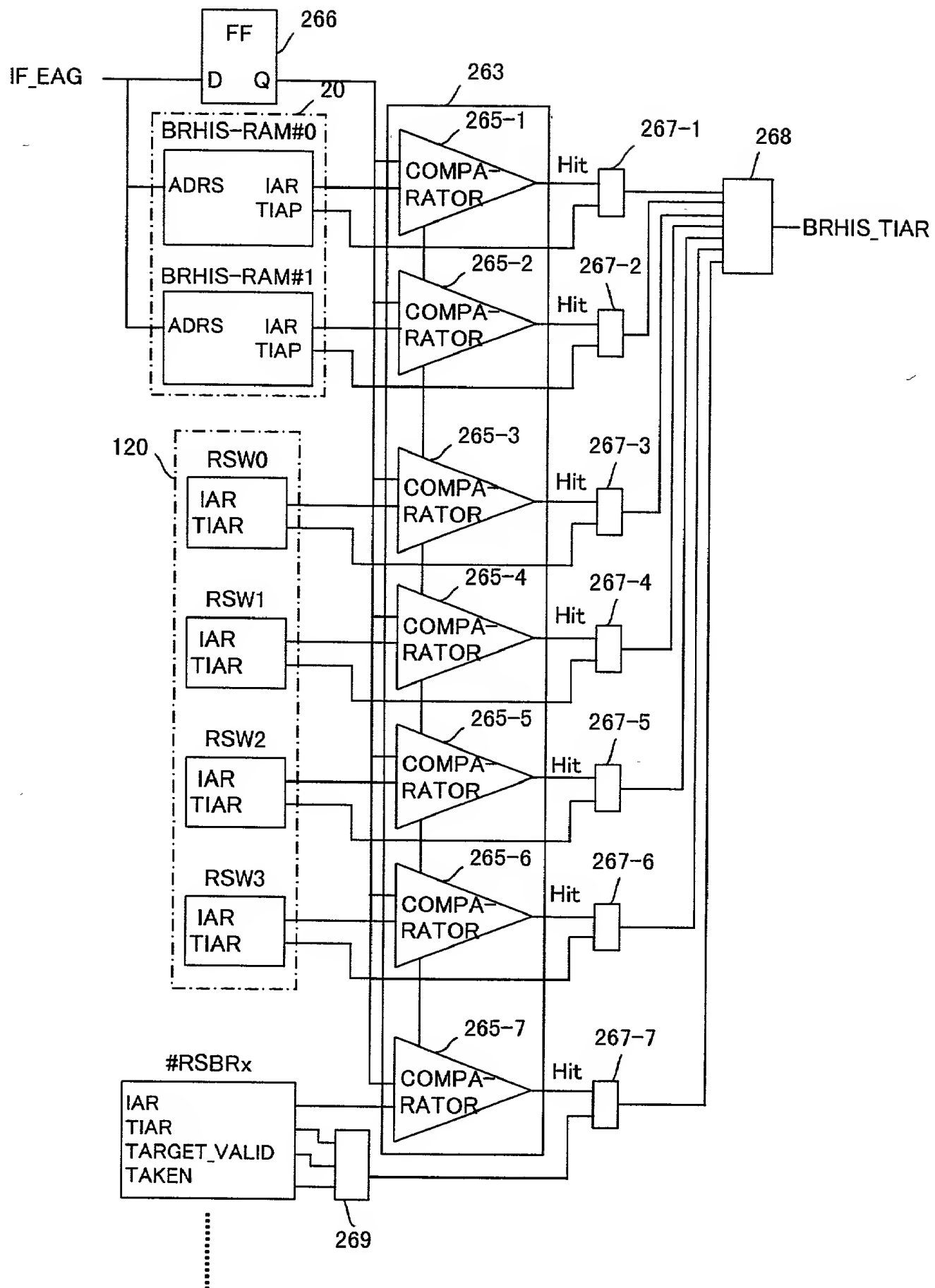


FIG. 29



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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

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As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

DEVICE AND METHOD FOR CONTROLLING

WRITING OF BRANCH HISTORY INFORMATION

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on _____
(if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されたとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

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Prior Foreign Application(s)

外国での先行出願

11-277816

(Number)

(番号)

Japan

(Country)

(国名)

(Number)

(番号)

(Country)

(国名)

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(Application No.)

(出願番号)

(Filing Date)

(出願日)

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(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

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I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

30th/September/1999

(Day/Month/Year Filed)

(出願年月日)

(Day/Month/Year Filed)

(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)

(出願番号)

(Filing Date)

(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)

(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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手続を米特許商標局に対して遂行する弁理士または代理人
として、下記の者を指名いたします。(弁理士、または代理
人の氏名及び登録番号を明記のこと)

James D. Halsey, Jr., 22,729; Harry John Staas, 22,010; David M. Pitcher, 25,908; John C. Garvey, 28,607; J. Randall Beckers,
30,358; William F. Herbert, 31,024; Richard A. Golthofer, 31,106; Mark J. Henry, 36,162; Gene M. Garner II, 34,172; Michael D.
Stein, 37,240; Paul I. Kravetz, 35,230; Gerald P. Joyce, III, 37,648; Todd E. Markotte, 35,269; Harlan B. Williams, Jr., 34,756;
George N. Stevens, 36,938; Michael C. Soldner, 41,455; Norman L. Ourada, 41,235; Kevin R. Spivak, P-43,148; and William M.
Schenler, 35,348 (agent)

書類送付先

POWER OF ATTORNEY: As a named inventor, I hereby appoint
the following attorney(s) and/or agent(s) to prosecute this
application and transact all business in the Patent and Trademark
Office connected therewith (list name and registration number)

Send Correspondence to:

STAAS & HALSEY
700 Eleventh Street, N.W.
Suite 500
Washington, D.C. 20001

直接電話連絡先: (名前及び電話番号)

Direct Telephone Calls to: (name and telephone number)

STAAS & HALSEY
(202) 434-1500

唯一または第一発明者名	Full name of sole or first inventor		
	Masaki UKAI		
発明者の署名	日付	Inventor's signature	Date
		Masaki Ukai	March 1, 2000
住所	Residence		
	Kanagawa, Japan		
国籍	Citizenship		
	Japan		
私書箱	Post Office Address		
	c/o FUJITSU LIMITED, 1-1, Kamikodanaka		
	4-chome, Nakahara-ku, Kawasaki-shi,		
	Kanagawa 211-8588, Japan		
第二共同発明者	Full name of second joint inventor, if any		
第二共同発明者	日付	Second inventor's signature	Date
住所	Residence		
国籍	Citizenship		
私書箱	Post Office Address		

(第三以降の共同発明者についても同様に記載し、署名をす
ること)

(Supply similar information and signature for third and subsequent
joint inventors.)